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Effects of On-Chip Capacitor on Switching Noise and Radiated Emission

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Introduction

With increasing clock frequencies of CMOS VLSIs, switching noise and electromagnetic radiation are becoming serious problems. Simultaneous switching noise (SSN) is induced by transient current of CMOS circuits due to the parasitic inductance of package. The characteristics of SSN have been investigated by many authors [1]-[4]. Radiated emission, i.e. electromagnetic interference (EMI) is another sensitive electromagnetic phenomenon whose radiation mechanism must be made clear in conjunction with LSI design, package structure design, and PCB wiring design in a system environment [5],[6].

In this paper, two types of test chips have been developed for evaluating switching noise and radiated emission. One has no intentional on-chip capacitance , the other has on-chip capacitance. The effects of on-chip capacitance on the SSN and radiated emission have been investigated by operating I/O circuits or core logic circuits.

Test Chip

Two types of test chips which generate switching noise and radiated emission were fabricated in a CMOS standard cell with 0.25 micron process technology. One had no intentional on-chip capacitance between the Vdd line and the ground line, the other had intentional on-chip capacitance of around 20 nF for the core logic circuits and around 30 nF for the I/O buffer circuits. Table 1 shows the common specifications of the two test chips. The die size was 10.4 × 10.4 mm. The developed chips were housed in a QFP with 256 I/O pins. The same I/O buffer circuits and core logic circuits were designed as noise generation sources for both chips. Fig. 2 shows the common schematic diagram of the test chips. The core logic circuits were arranged in a 3 by 3 matrix. Each unit has two types of logic circuits: D-type flip-flop (D-F/F) circuits and buffer chain circuits. The I/O buffer circuits with three different current drivabilities, which are defined by the guaranteed value of I_{OL} were arranged at each side of a chip. They were 4mA driver, 8mA driver, and 16mA driver respectively. The signals for controlling the operation were allocated at the rest side of a chip.

Measurement

An evaluation board with 6 conductive layers was designed. The size was 200 × 200 mm. The three groups of signal line traces for each type of I/O buffer circuits were arranged in a stripline structure at around the test chip. The developed test chips were controlled by either external switches or a personal computer (PC). The radiated emission was measured by using a developed probe scanning system with a probe head which moves in the X, Y, Z, and theta directions.

Fig.2 (a) shows the magnetic near field distribution on the surface of the QFP for the chip without on-chip capacitance when core logic circuits switched at a frequency of 50 MHz. Fig.2 (b) shows the magnetic field for the one with on-chip capacitance. In this case, 2048 stages of D-F/F circuits were activated for each unit of core circuits. Lower level of radiated emission was observed for the chip with on-chip capacitance. The peak of radiated spectrum was reduced by approximately 5 dB

The switching noise was measured using a sampling oscilloscope. Fig.3 shows signal waveforms (upper traces) and simultaneous switching noises (lower traces) for the case when 31 output buffers of 8 mA drivability switched simultaneously. Fig.3(a) is for the chip without on-chip capacitance, and Fig.3(b) is for the one with on-chip capacitance. The output signals were a half of clock frequency of 30 MHz.

The ground bounce swung to the direction opposite to signal direction at first transient for the chip with on-chip capacitance, whereas the ground bounce swung to the positive direction at both rising edge and falling edge for the one without on-chip capacitance. For signal waveforms, rising edge was degraded for without on-chip capacitance, while overshoots and undershoots were observed for with on-chip capacitance. These overshoots resulted in larger radiated emission compared with that for the chip without on-chip capacitance. Fig.4 shows a schematic illustrating the behavior of switching noise due to the existence of on-chip capacitance.

Summary

Two types of test chips have been developed for evaluating the effects of on-chip capacitance on

simultaneous switching noise and radiated emission by switching I/O circuits or core logic circuits. Radiated emission was reduced by approximately 5 dB due to on-chip capacitance for the core logic operation, while the peak noise level of switching noise and resultant radiated emission were increased due to on-chip capacitance for the I/O circuit operation. The rising edge of signal was degraded without on-chip capacitance for low drivability buffers. The above results showed larger on-chip capacitance does not always provide better performance of SSN and EMI. In particular, the optimum design of on-chip capacitance is required for I/O circuits.

Acknowledgements

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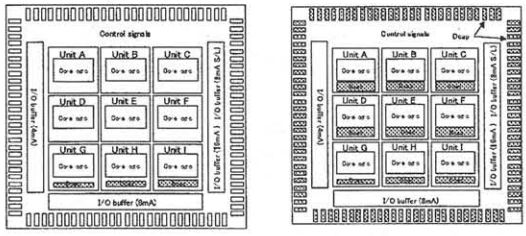
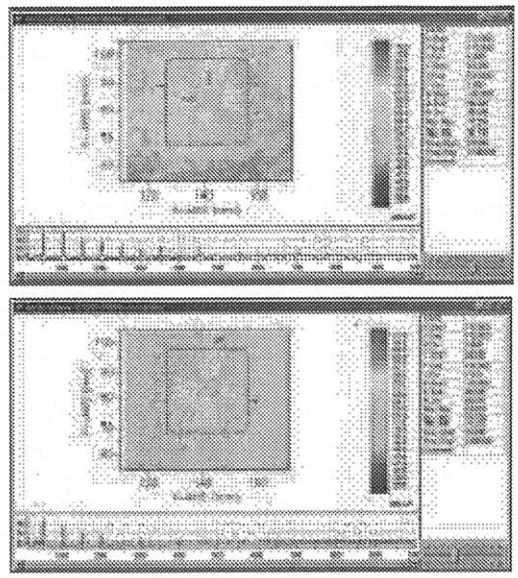
Table 1 Test chip specification

Process	CMOS, 0.25um, 3 level metal layers
Design	standard cell
Chip size	10.4 × 10.4 mm
Package	QFP (Quad Flat Package)
I/O count	256 pins
Power supply	Separation of I/O V_{DD} from Core V_{DD}



(a) without on-chip capacitance (b) with on-chip capacitance

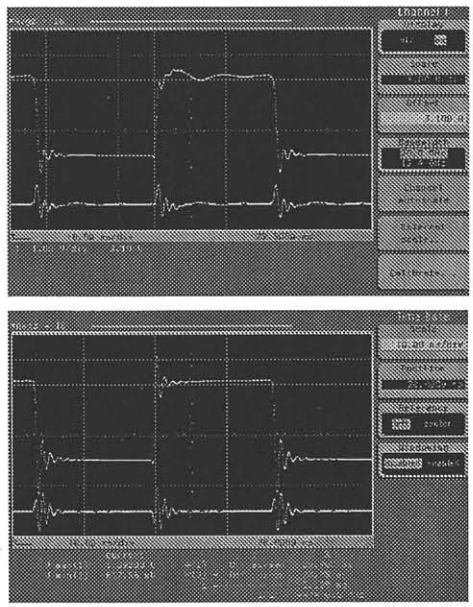
Fig.1 Configuration of test chips



(a)

(b)

Fig.2 Magnetic near field for core logic operation: (a) without , (b) with on-chip capacitance



(a)

(b)

H: 1V/div
V: 10ns/div

Fig.3 Switching noises and signal waveforms for 30 buffers switched simultaneously: (a) without, (b)with on-chip capacitance

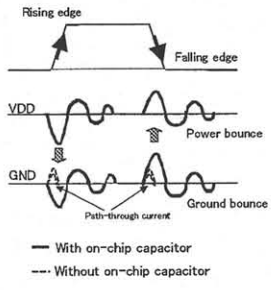


Fig.4 Behavior of switching noise