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GHz Clock Distribution Using Transmission Line Interconnect and CMOS Differential Driver Circuit in Si ULSI

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1. Introduction

For GHz signal propagation through long interconnect in a cm-order Si ULSI chip such as clock distribution and bus line data transmission, signal transmission through the distributed constant circuit is inevitable. In this paper, we propose a circuit configuration using the H-tree transmission line and show that the use of transmission lines with relatively large characteristic impedance of 100Ω is desirable because of less degradation of waveform and signal delay due to resistance loss.

2. H-Tree Configurations and Circuit Design

The H-tree configuration is known for being able to minimize a clock skew at each receiver [1]. Figure 1 shows a typical 2-stage H-tree configuration. In an *i*-stage H-tree, a square chip is divided into 4^i sub-cells. When one uses the transmission line, the impedance matching is substantial, *i.e.*, each transmission line should have different characteristic impedance as shown in Fig. 1. When pair-line transmission is used, the metal width should be decrease so as to increase the characteristic impedance under the condition of constant insulator thickness. A relatively small cross-section metal line requires the design difficulty of the line with arbitrary characteristic impedance. From this viewpoint, we propose the H-tree configuration with repeaters as shown in Fig. 2. Using the repeater driver (***Driver-2*** in Fig. 2), an infinite increase in characteristic impedance is eliminated.

As the transmission line interconnect, the pair-line structure is a possible candidate because the pair-line structure can be implemented using upper 2 layers of multilevel interconnect. If the ideal TEM mode is assumed, the cross-sections of 50Ω- and 100Ω-lines are shown in Fig. 3. In over GHz condition, a skin depth is μm-order; the line resistance is not negligible as compared with the value of the characteristic impedance.

For driving the pair-line, 0.3μm CMOS differential circuit is used in this work as shown in Fig. 4. The load resistance (R_{out}) varies the output impedance of differential circuit. In the input terminal of ***Driver-2*** and ***Receivers*** of Fig. 2 are terminated in parallel by the resistor that has the same resistance as the characteristic impedance of the line. Circuit parameters are summarized in Table 1.

3. Results and Discussion

Figures 5 and 6 show SPICE simulation results of the input and output signal waveforms. The characteristic impedance (Z_o) of the line is 50Ω and 100Ω. With increase in the resistance loss, the delaytime and output waveform are degraded. The waveform degradation is due to the decrease of the signal swing and dispersion of the line; the degrease of signal swing through the lossy transmission line is proportional to $\exp(-R_{Loss}l/2Z_o)$, where R_{Loss} and l are resistance per unit length and length of the line, respectively.

When the resistance loss is 15Ω/cm, the degradation of delaytime and waveform is negligible. Figure 7 shows 90%-delaytime, $\tau_{90\%}$. In the 50Ω-case, the degradation of $\tau_{90\%}$ is larger than that in the 100Ω-case; this is because of the relatively large signal swing degradation and dispersion. In order to improve the degradation, R_{Loss} should be reduced. However, to decrease R_{Loss}, larger cross-section line is required, *i.e.*, a wide line of over 10μm is required. Too wide line is not realistic to be implemented using multilevel interconnect in LSI chip. So that, to decrease the degradation of waveform and delaytime, it is desirable to increase the characteristic impedance, *e.g.*, 100Ω.

For a chip with over-10GHz local clock, a sub-cell size should be small in order that the interconnect is designed based on the conventional RC-lumped model inside the sub-cell; a sub-cell size should be less than 500μm [2]. This requires the increase in the number of stages in H-tree. However, since the global clock is order of 3GHz even in the 2010-era, the 3rd or 4th H-tree with the length of less than mm can be designed based on the conventional CMOS inverter driver circuit. From this viewpoint, for the GHz clock distribution, we can propose the following configuration; (1) the 1st and 2nd H-tree is designed using transmission line and differential driver/receiver circuit, and (2) the 3rd and higher order stages is designed using the conventional RC-lumped interconnect and CMOS driver circuit.

3. Summary and Conclusion

We have discussed the GHz clock distribution using transmission line and differential driver/receiver circuit. In order to decrease the degradation of delaytime and output waveform, the large characteristic impedance such as over 100Ω is desirable. Furthermore, the H-tree configuration for a chip with 3GHz global and over-10GHz local clock has been proposed.

References

(1) For example, H. B. Bakoglu, "*Circuits, Interconnections, and Packaging for VLSI*", Addison-Wesley, 1990. W. Wolf, "Modern VLIS Design –Systems o Silicon", Prentice Hall PTR, 1998.
(2) K. Masu, IEICE Technical Report, 101(1) pp.87 (2001)

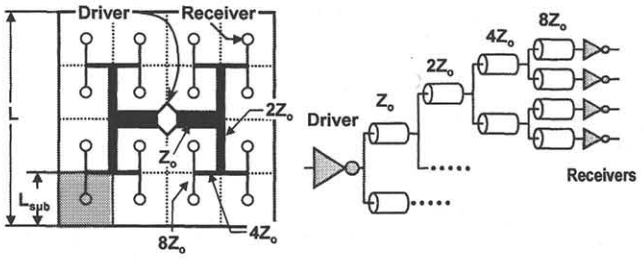

Fig. 1 H-tree configuration for clock distribution..

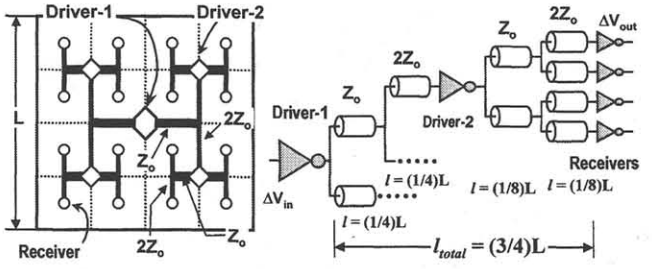

Fig. 2 H-tree configuration with repeater for clock distribution (This work)

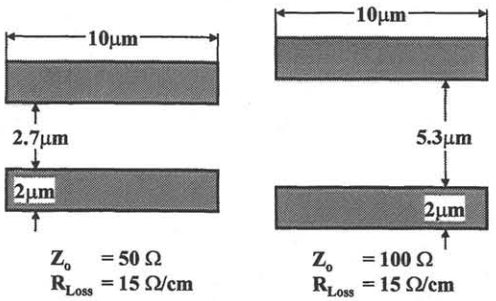

Fig. 3 Possible pair-line configuration (ideal case).

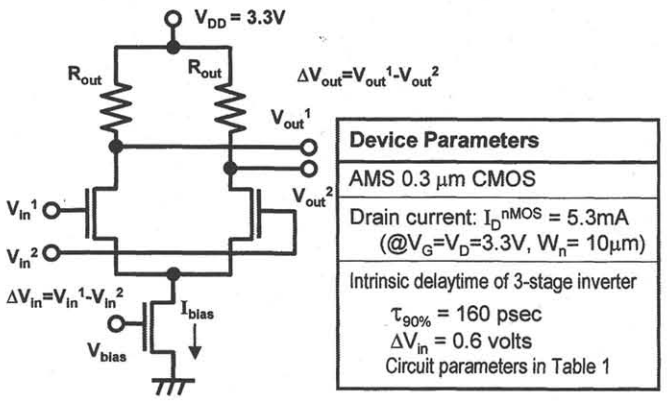

Fig. 4 Differential driver and receiver.

Table 1. parameters of Designed Circuit

	Z_o = 50Ω	Z_o = 100Ω
W_n and R_{out} of Driver-1	400μm / 50Ω	400μm / 100Ω
W_n and R_{out} of Driver-2	150μm / 50Ω	100μm / 100Ω
W_n and R_{out} of Receiver	100μm / 50Ω	100μm / 250Ω

W_n: Gate width of nMOS, R_{out}: see Fig. 4,
Z_o: Characteristic impedance of the line (see Fig. 2)
I_{bias} : Designed value is ≈10mA.
ΔV Signal swing is designed to be 0.6V.

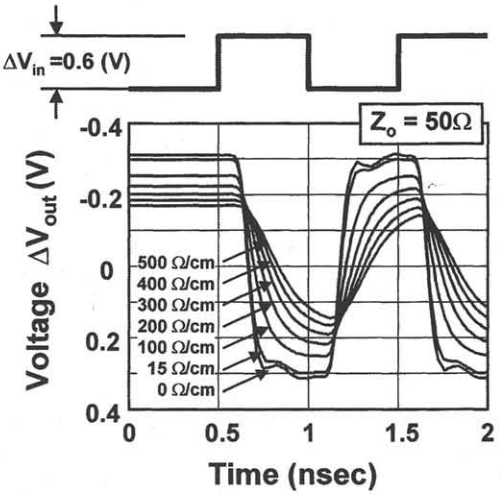

Fig. 5 Input and output signal waveform of receiver. L =16mm and Z_o = 50Ω in Fig. 2. [Simulation]

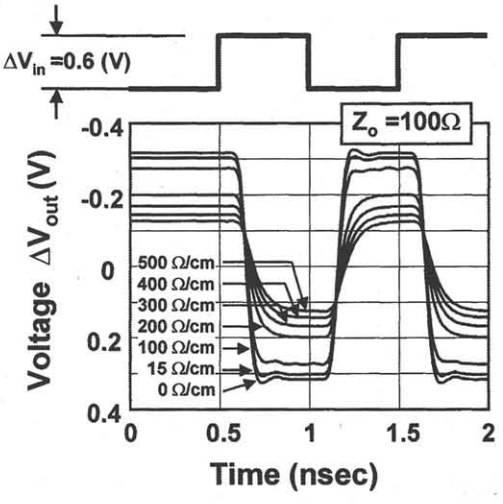

Fig. 6 Input and output signal waveform of receiver. L =16mm and Z_o = 100Ω in Fig. 2.[Simulation]

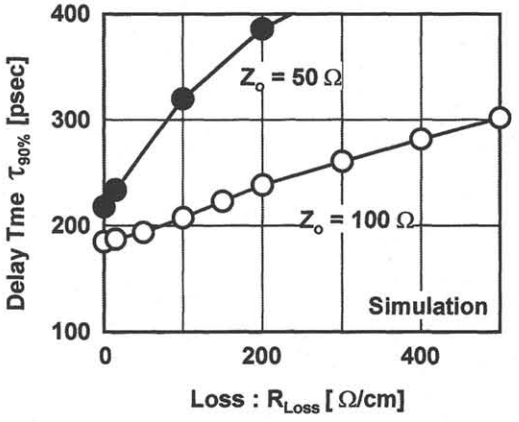

Fig. 7 90%-delaytime as a function of R_{Loss}.

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