Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 198–199

B-3-2

High-Resolution Stress Mapping of 100-nm Devices Measured by Stress TEM

Masanari Koguchi, Kuniyasu Nakamura and Kaoru Umemura
Central Research Laboratory, Hitachi Ltd., 1-280 Higashi-Koigakubo, Kokubunji, Tokyo 185-8604, Japan
Phone: +81-42-323-1111 Fax: +81-42-327-7677
E-mail: Masanari-crl.Koguchi@c-net3.crl.hitachi.co.jp

1. Introduction

There are many stress fields under the gate and plug of CMOS and other Si devices. Especially near the STI walls, STI corners, and the interface of the Si and SiN, high stress causes many failures. Stress causes defects among other problems, and these defects attract contamination, thus generating a junction leakage current. Stress also changes the band-gap, and this causes fluctuation in current characteristics. To achieve an anti-stress process, we have to manage internal stress by using precise measurements. We propose a new method, *"Stress TEM"*, for measuring the internal stress of a Si substrate and explain some effective applications to counter stress.

2. Methods

We applied the nano-diffraction method shown in Fig. 1, to stress measurement by using a transmission electron microscope (TEM). We used a 300-kV TEM with a field-emission (FE) electron gun, because a FE-gun can make a small and parallel probe, which is necessary to reduce diameter of diffraction spots. We can also make parallel probes 10 nm in diameter with irradiation angles of 0.4 mrad using this device. Stress is relaxed in a thin specimen, so high-energy-beams are advantageous for observing thick specimens. The pixel number of the electron detector directly corresponds to the resolution of stress, so we used a high-resolution CCD camera with a scintillator to convert the electrons to photons.

The principle of our stress-TEM method is shown in Fig. 2. In the crystalline specimen, the electron beam is diffracted and a diffraction pattern is generated. The spacing of these spots corresponds to the lattice spacing. Under tensile stress, such as that depicted in this figure, the spacing is decreased. Here, standard lattice spacing is defined as d, and the shift caused by the stress is Δd, so the strain is simply $\Delta d/d$. Thus, stress is described by formula (A) in Fig. 1.

Almost 30 nano-diffraction patterns were observed for a sample. The horizontal and vertical spacing of the spots were calculated for a pattern. D was measured from the diffraction pattern of the substrate, and Δd was measured as the difference between d and the lattice spacing of the measured position. The sensitivity of this technique was almost 0.05% for the amount of strain and 75 MPa for the amount of stress.

This method has an advantage over conventional techniques such as the CBED-EELS method, because it is applicable to thick specimens (>0.3 μ m) and easy to quantify [1-3]. Thick specimens are necessary to minimize the stress-relaxation caused by the thinning of sample preparation.

3. Results

Two-dimensional stress mapping of stressed bits in memory is shown in Fig. 3. Specimen thickness was 0.3 μ m. From the analyzed data of the strain, we drew the stress contour lines on the image. A comparison of stressed and unstressed bits is shown in Fig. 4. In the stressed bit, there are some defects in the substrate that gave it slow read/write characteristics. The maximum stress amounted to more than 2000 MPa. In the unstressed bit, stress was less than 500 MPa. We frequently found in this study that stress had a strong relation with the electronic characteristics of the device. Thus, we can say that stress management is very important for controlling quality of many kinds of devices.

4. Conclusions

We used the nano-diffraction method of TEM to investigate the 2D-stress distribution of devices, and achieved a resolution of 10 nm and a sensitivity of less than 100 MPa. The stress-TEM method has sufficient sensitivity and resolution for the stress management of 100- nm-devices.

Acknowledgments

We are grateful to Mr. Masataka Kato, Dr. Shinichiro Kimura and Mrs. Ruriko Tsuneta of Hitachi Ltd. for supplying the specimens and for making useful suggestions. We also thank Dr. Toshiaki Yamanaka and Dr. Shinichi Tachi for supporting our research.

References

[1] D. B. Williams and C. B. Carter *Transmission Electron Microscopy*, 301-345 (1996) Plenum Press (New York)

[2] K. Kimoto and M. Tanaka, Jpn. J. Appl. Phys. **32**, 211 (1993)

[3] A. Toda, N. Ikarashi and H. Ono, J Crst. Growth **210**, 341 (2000)

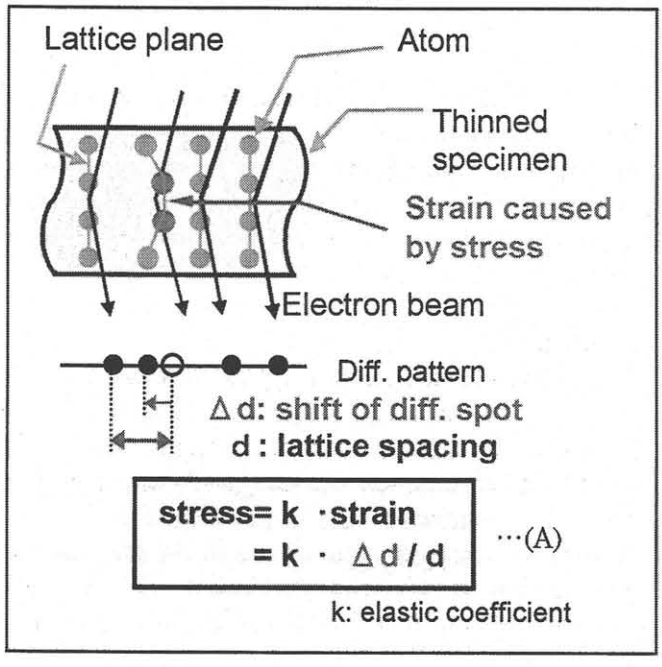

Fig. 1 Measurement of stress using nano-diffraction pattern of electron beam

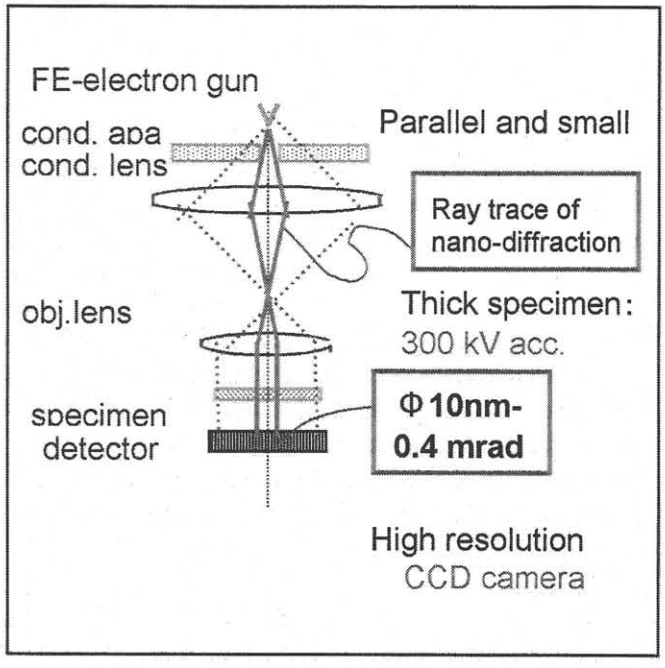

Fig. 2 Principle of nano-diffraction method

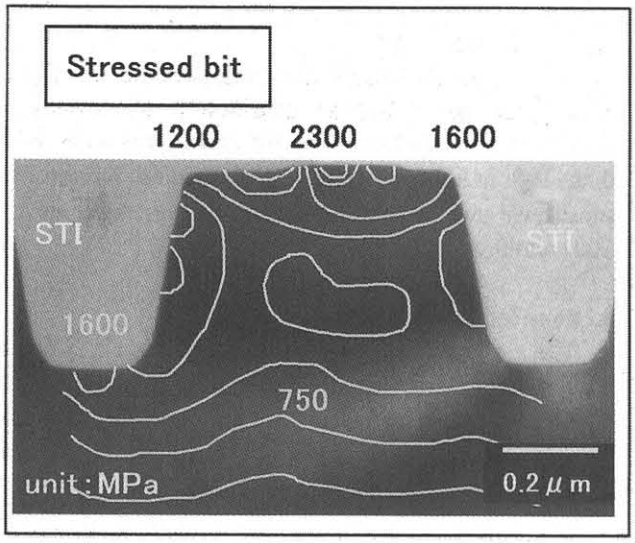

Fig. 3 Stress mapping of memory

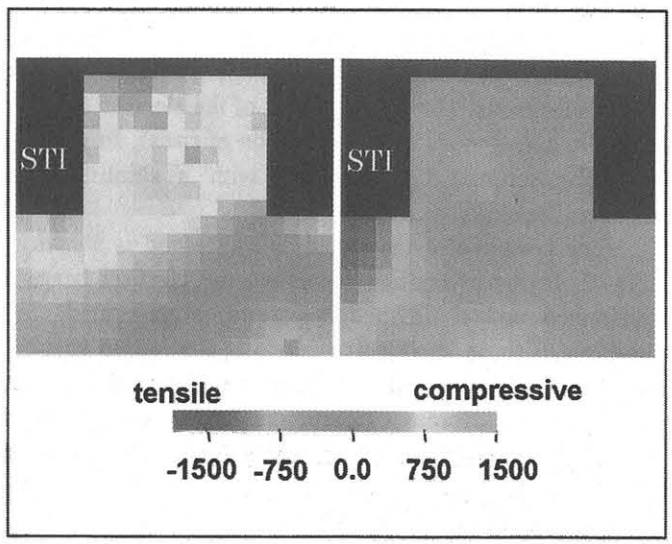

Fig. 4 Stress mapping of stressed/unstressed bits of memory