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A Decoupled Capacitance Measurement Technique for Characterization of Small-Geometry MOSFETs with Ultra-Thin Gate Oxides

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1. Introduction

Capacitance-voltage (C-V) measurement is a fundamental and essential technique for MOSFET device characterization such as oxide thickness determination [1-2] and effective and metallurgical channel length extraction [3-4]. It is therefore crucial to accurately determine the device capacitances; however, accurate capacitance measurement has become increasingly difficult due to several issues resulted from aggressive scaling of CMOS technology. Issues include capacitance roll-off caused by gate leakage current and overestimated channel capacitance due to parasitic capacitances.

The leakage-related capacitance degradation has been extensively studied [2,5] and could be overcome by using a test structure with channel length around 1 μm. However, the parasitic capacitance becomes significant as channel length is reduced, and moreover it's sensitive to the geometrical structure of a test structure. This work presents a practical C-V measurement technique to decouple the channel capacitance (in both inversion and accumulation modes) from parasitic capacitances, which is confirmed by process/device simulation.

2. Decoupled Capacitance Measurement Technique

The technique is demonstrated through an NMOSFET of multi-finger structure, as shown in Fig. 1. For each finger, the length and width are 1 μm and 34 μm, respectively, and there are 60 fingers connected together (not shown) to increase the signal level during measurement. Moreover, all the measurements were performed using a HP4284 LCR meter in parallel mode with a signal frequency of 100 kHz and a test signal of 20 mV. Fig. 1 also shows the parasitic capacitances [6]. C_J is the junction capacitance caused by the depletion charge between S/D and substrate, C_{STI} is the STI capacitance associated with the overlap between gate and STI, and C_{ov} is the overlap capacitance between gate and S/D. C_{ov} basically consists of three components: direct overlap capacitance C_{do}, outer fringe capacitance C_{of}, and inner fringe capacitance C_{if}. It should be noted that only C_{do} and C_{of} are present when the surface is *strongly* inverted or accumulated because the inversion or accumulation layer shields the inner fringe component [6,7].

The C-V measurement is customarily performed using the setup shown in Fig. 2(a), and its experimental result is shown in Fig. 3(a). One drawback for this setup lies in the fact that some parasitic capacitances such as C_{of}, C_{do} and C_{STI} are included in the measurement, overestimating the accumulation channel capacitance (C_{acc}) and inversion channel capacitance (C_{inv}), which becomes increasingly significant when devices are aggressively scaled.

On the other hand, an improved setup and its C-V curve are shown in Fig. 2(b) and 3(b), respectively. The use of this setup is to shunt away some parasitic capacitances from measurement. That is,

$C_{measured}$ (@$V_G = V_{dd}$, inversion) = $C_{of} + C_{do} + C_{inv}$, (1a)

$C_{measured}$ (@$V_G = 0$ V) = $C_{ov} = C_{of} + C_{do} + C_{if}$, and (1b)

$C_{measured}$ (@$V_G < 0$) = $C_{of} + C_{do}' + C_{if}'$ (1c)

where C_{do}' is equal to or less than C_{do} because accumulation layer reduces the *effective* overlap l_{ov}, and C_{if}' is between 0 and C_{if} until some *critical* point is reached at which the accumulation layer *completely* shields this component. Although some parasitic capacitances still appear in Eq. (1), C_{inv} and C_{acc} could be obtained by further using the measurement configuration shown in Fig. 2(c) and the proposed algorithm schematically illustrated in Fig. 5.

As shown in Fig. 2(c), the gate is connected to the HI terminal, the substrate is connected to the LO terminal, and the source/drain is grounded which bypasses C_{inv} and C_{ov}. As a result, the capacitance measured in the inversion mode is C_{STI}, while that measured in the accumulation mode is the sum of C_{STI} and C_{acc}. Therefore, through this setup, C_{acc} can be obtained by simply subtracting the capacitance measured in the inversion mode from that measured in the accumulation mode, and Fig. 4 shows the measurement result. In other words,

$C_{acc} = C_{measured}$ (@accumulation) – $C_{measured}$ (@inversion) (2)

Moreover, C_J can be obtained by the use of the measurement setup shown in Fig. 2(d).

Next, a method is proposed for the first time to separate C_{if} from C_{ov}. Fig. 5 shows the enlarged C-V curve of Fig. 3(b) in the accumulation mode (i.e. $V_G < 0$), which can be approximated by two lines with different slopes. It's speculated that the decrease in capacitance along the line AB is mainly due to the formation of the accumulation layer that gradually shields the inner fringe component, while the decrease in capacitance along the other line is mainly due to the reduced overlap between S/D and gate that is depleted more as V_G increases further. Hence, the intersection of these two lines can be approximately regarded as the *critical* point where C_{if} vanishes. Namely,

$C_{if} = C_{measured}$ (@$V_G = 0$ V) – $C_{measured}$ (@critical point) (3)

From Fig. 5, C_{if} is equal to 2 pF, whose contribution to the total overlap capacitance of 3.5 pF is consistent with the theoretical calculation [6]. Moreover, C_{inv} is found to be 28.8 pF by substituting C_{if} into Eq. (1). The proposed method is further verified through process/device simulation, as shown in Fig. 6.

One important application of this technique is to more accurately calculate the electrical oxide thickness (T_{inv}) and oxide thickness including quantum-mechanical effect (T_{qm}) [1] by using C_{inv} and C_{acc}, respectively. For example, using this proposed technique, together with Fig. 3(b) and Fig. 4, T_{inv} is 2.4 nm and T_{qm} is 1.5 nm. However, if the traditional C-V measurement, i.e. Fig. 2(a) and Fig. 3(a), is used, T_{inv} and T_{qm} become 2.1 nm and 1.3 nm, respectively.

3. Summary

A practical C-V measurement technique is proposed, which is capable of separating the parasitic capacitances from the traditional C-V measurement as well as the inner fringe capacitance (C_{if}) from the overlap capacitance (C_{ov}). It's also shown that, compared to this proposed technique, using the traditional C-V measurement may result in a significantly thinner oxide thickness.

References

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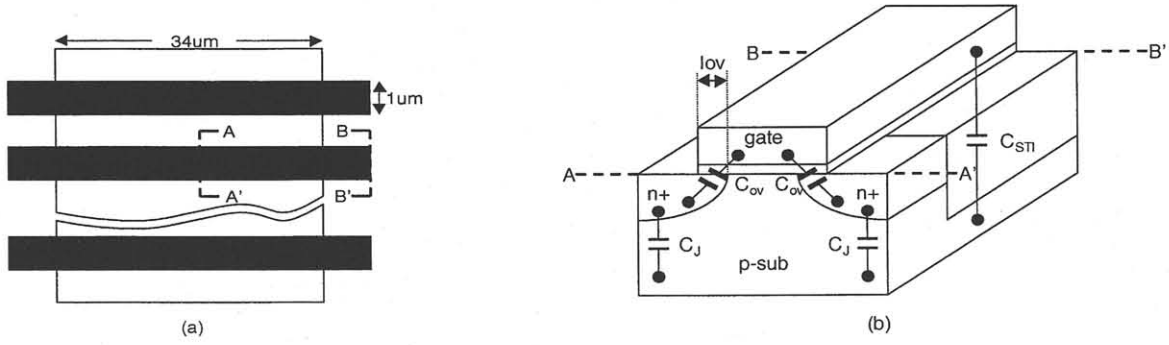

Fig. 1. (a) Top view of the test structure (not to scale) in the study. (b) Cross section (not to scale) along AA' & BB' and associated parasitic capacitances.

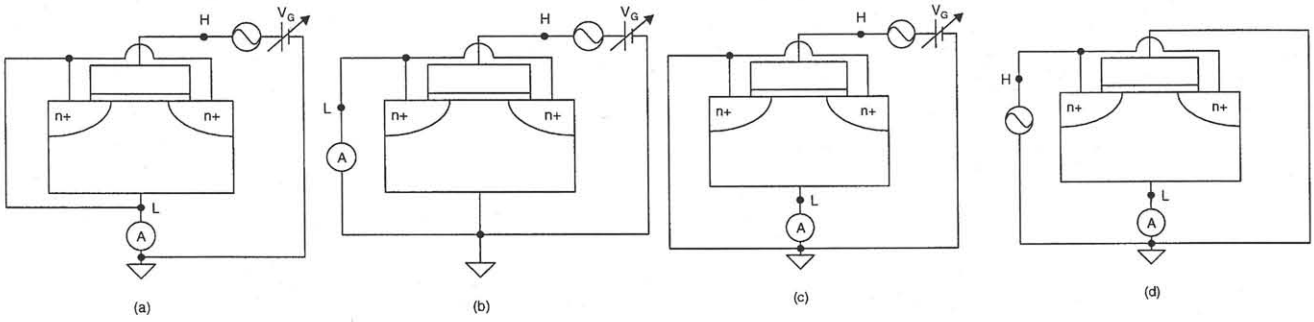

Fig. 2. (a) Measurement configurations used in this work. Here, H and L represent the "HI" and "LO" terminals, respectively, of a HP4284 LCR meter.

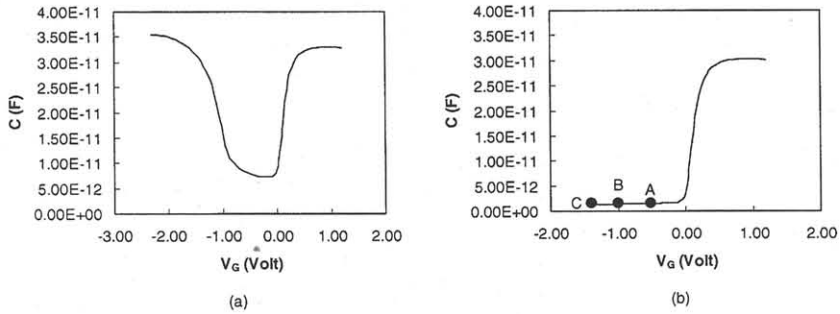

Fig. 3. High frequency C-V curves measured using the setup shown in Fig. 2(a) and 2(b).

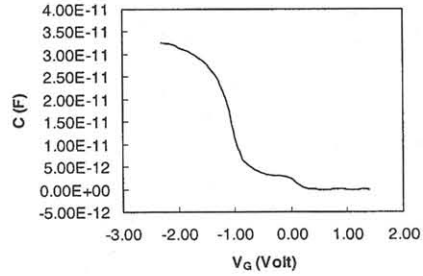

Fig. 4. C_{acc} obtained by subtracting the capacitance measured in inversion mode from that measured in accumulation mode of Fig. 2(c).

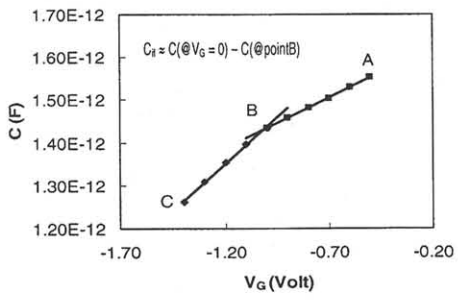

Fig. 5. The curve AC in Fig. 3(b) is displayed in an enlarged scale.

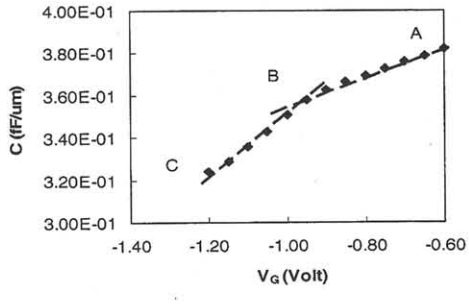

Fig. 6. Simulated result verifies the validity of the proposed method.