

B-3-4**Extraction of Interface State Density in Ultra-Thin Gate Dielectrics: A Composition Method of Ideal CV Curves in High-Frequency CV Analysis**

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1. Introduction

We propose a new method to construct ideal CV curves in ultra-thin gate dielectrics, and demonstrate its effectiveness in extracting interface state density in high-frequency CV analysis. As ITRS dictates, current CMOS technologies demand gate insulators with higher dielectric constants relative to SiO₂. Many of high-k dielectrics, however, are expected to show a large amount of interface states due to high average coordination number of constituent atoms [1]. Therefore precise characterization of interface states is crucial for future ultra-thin gate dielectrics. Among the CV methods for the evaluation of interface states [2], low-frequency measurements are difficult to implement because of large leakage current across ultra-thin gate dielectrics. Thus, the only viable option in CV methods is high-frequency CV (HF-CV) where a measured HF-CV curve is compared with an ideal curve. Although a simple analytical expression can be used for ideal C-V curves in thick gate dielectrics [2], it is not applicable to ultra-thin films due to quantum mechanical effect in a Si substrate [3]. We propose instead a new method to compose an ideal CV curve for ultra-thin gate dielectrics. The evaluations of interface state density based on this method are performed on ultra-thin silicon oxynitride and ZrO₂/Zr-silicate.

2. Analysis Method of Interface State Density

In Fig 1 we show the equivalent circuit of an MIS capacitor with an ultra-thin gate dielectric. The essence of the proposed method is that the ideal CV curves for gate dielectrics with any effective thickness is composed from C_s(E_{ox}) and φ_s(E_{ox}) relations of a Si substrate. Ideal CV curves are expressed as

$$1/C = T_{\text{eff}}/\epsilon_{\text{ox}} + 1/C_s(E_{\text{ox}}) \quad (1)$$

$$V_g = E_{\text{ox}} T_{\text{eff}} + \phi_s(E_{\text{ox}}) + V_{\text{fb}} \quad (2)$$

where E_{ox} is effective (i.e. SiO₂ equivalent) electric field across a gate dielectric, and T_{eff} and V_{fb} are effective thickness and flatband voltage, respectively. ε_{ox} is dielectric constant of SiO₂.

We extracted C_s(E_{ox}) and φ_s(E_{ox}) relations from the CV measurements on thermal SiO₂ films. Since thermal SiO₂ has negligible interface state density, the CV curves reconstructed from eqs.(1) and (2) can be used as an ideal CV curve. (Although CV simulations may also be used to extract C_s(E_{ox}) and φ_s(E_{ox}) relations, one has to be careful with the discrepancy in accumulation capacitance among different simulators [4].) We measured CV curves of SiO₂ on MOS capacitors with a p-type Si substrate. The substrate

impurity concentration was nearly equal to that of the samples under evaluation. The impurity concentration in the n⁺ polysilicon gate was high enough to disregard gate depletion (>3x10²⁰cm⁻³). In Fig 2 we show C_s(E_{ox}) and φ_s(E_{ox}) relations derived from

$$1/C_s = 1/C - T_{\text{phys}}/\epsilon_{\text{ox}} \quad (3)$$

$$\phi_s = V_g - E_{\text{ox}} T_{\text{phys}} - V_{\text{fb}} \quad (4)$$

The physical thickness (T_{phys}) was obtained from cross sectional TEM. The effective electric field E_{ox} was evaluated from charge density (eq. (5)).

$$\epsilon_{\text{ox}} E_{\text{ox}} = \int_{V_{\text{fb}}}^{V_g} C(V_g') dV_g' \quad (5)$$

In addition to the experimental C_s(E_{ox}) and φ_s(E_{ox}) relations, we also show those derived from the analytical model [2] in Fig. 2. The analytical model is inaccurate in accumulation regime (E_{ox} > 0), leading to large inaccuracies in evaluated interface state density.

The energy distribution of interface states is derived as follows. First, the effective thickness of a gate dielectric under evaluation is determined by adjusting T_{eff} and V_{fb} in ideal CV curves (eqs.(1) and (2)), so that the saturation properties in accumulation capacitance are well reproduced. Second, V_g-φ_s relations are derived for both the evaluated sample and the ideal CV curve. In the evaluated sample, C_s is derived from 1/C_s = 1/C - T_{eff}/ε_{ox}. The surface potential φ_s corresponding to C_s is derived from C_s(E_{ox}) and φ_s(E_{ox}) relations in Fig.2, together with E_{ox} in the ideal CV curve. The gate voltage of the ideal CV curve is then derived from eq. (2). Thus, a set of values (φ_s, V_g(evaluated), V_g(ideal)) are obtained. The energy distribution of interface states is obtained as D_{it} = (ε_{ox}/qT_{eff})([dV_g/dφ_s]_{evaluated} - [dV_g/dφ_s]_{ideal}).

We evaluated D_{it} of a silicon oxynitride film with high nitrogen concentration (Figs. 3 and 4). Significant density of interface states is observed near the valence band edge, consistent with a previous report on PECVD silicon nitride films [5]. As another example, we show the evaluation of N_{it} (cm⁻²) for ZrO₂/Zr-silicate film (T_{eff} = 0.98nm) in Fig.5.

3. Conclusions

We have proposed a composition method of ideal CV curves for ultra-thin gate dielectrics, and demonstrated its ability to evaluate interface state density. The proposed method can be applied to ultra-thin gate dielectrics where the analytical model for an ideal CV curve is invalid due to quantum mechanical effect. We have also confirmed that the interface state density near the accumulation band edge is accurately determined with this method.

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References

- 1) G. Lucovsky, Y. Wu, H. Niimi, V. Misra, J. C. Phillips, Appl. Phys. Lett. **74**, 2005 (1999).
- 2) See for example: E. H. Nicollian and J. R. Brews, "MOS Physics and Technology," John Wiley & Sons, New York (1982).
- 3) S. Takagi and A. Toriumi, IEEE Trans. Electron Devices **42**, 2125 (1995).
- 4) C. A. Richter, A. R. Hefner and E. M. Vogel, IEEE Electron Device Lett **22**, 35 (2001).
- 5) V. Misra, H. Lazar, M. Kulkarni, Z. Wang, G. Lucovsky and J. R. Hauser, Mat. Res. Soc. Symp. Proc. **567**, 89 (1999).

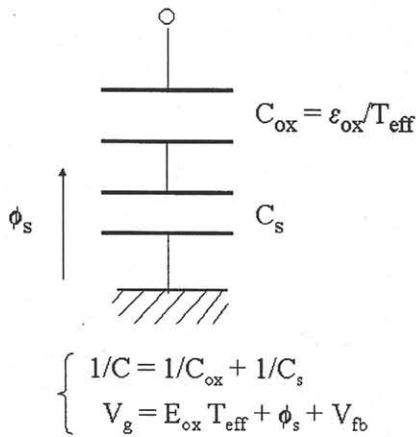


Fig. 1 Equivalent circuit for MIS capacitors with an ultra-thin gate dielectric. Ideal CV curves are constructed from experimentally obtained $C_s(E_{ox})$ and $\phi_s(E_{ox})$ relations.

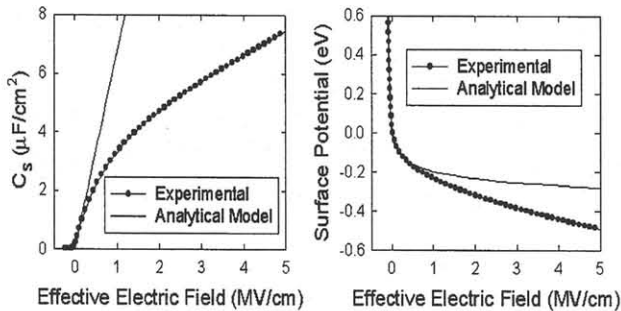


Fig. 2 Accumulation capacitance C_s and surface potential ϕ_s as a function of E_{ox} (circles). The data were experimentally obtained from 3.4-nm thermal SiO_2 . $C_s(E_{ox})$ and $\phi_s(E_{ox})$ relations for analytical model [2] are also indicated (solid curves).

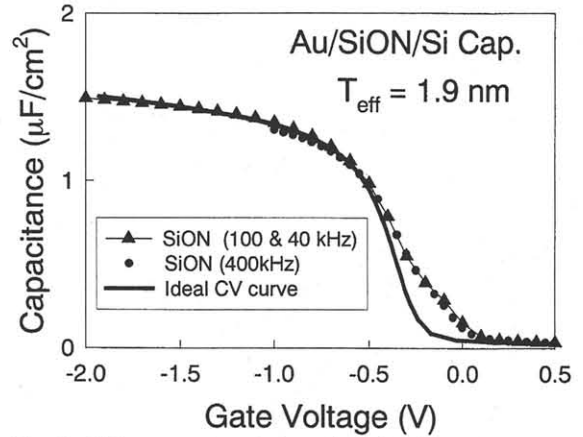


Fig. 3 CV curves of an Au/oxynitride/p-Si capacitor and the "ideal" CV curve composed from experimental CV data of SiO_2 . The CV curves of oxynitride at different frequencies are in agreement, indicating the acquisition of a proper "high-frequency" CV curve.

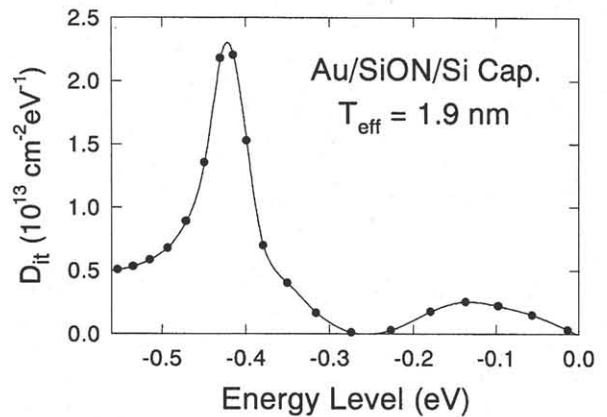


Fig. 4 Energy distribution of interface states for an oxynitride film with $T_{eff} = 1.9$ nm derived from the CV curve (400kHz) in Fig. 3. The D_{it} distribution from the midgap (0eV) to the valence band edge (-0.56eV) is shown.

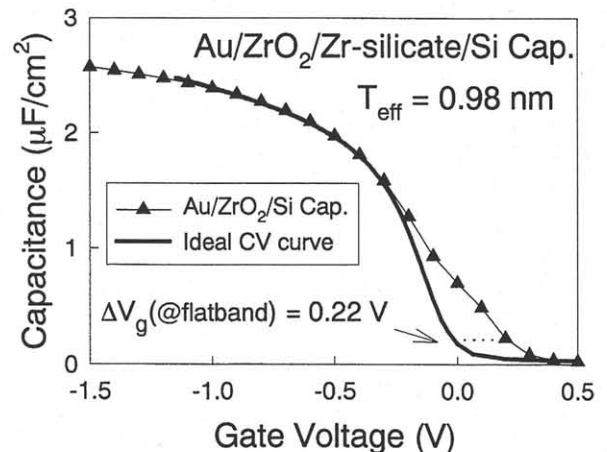


Fig. 5 The CV curve of Au/ ZrO_2 /Zr-silicate/Si capacitor and ideal CV curve ($T_{eff} = 0.98$ nm). The interface state density between the valence band edge and the flatband condition is $N_{it} = (\epsilon_{ox}/qT_{eff})\Delta V_g = 4.8 \times 10^{12} \text{cm}^{-2}$.