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## Enhanced Negative-Bias-Temperature Instability of P-Channel MOSFET by Plasma Charging Damage

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### 1. Introduction

Negative-bias-temperature instability (NBTI) represents one of major reliability concerns for deep sub-micron PMOS transistors [1] ~ [4]. Recently, it was shown that the plasma charging damage could potentially worsen the situation [5]. However, more detailed information, such as the effects of antenna size, charging polarity, and the device location on the wafer, is still lacking. In this study, we address these issues by fabricating and characterizing antenna devices. Some interesting results were obtained, which would help clarify the role of plasma charging in affecting the NBTI characteristics of PMOS transistors.

### 2. Experimental

P-channel MOS transistors with p<sup>+</sup> poly-Si gate were fabricated on 6-inch wafers. Gate oxide thickness was 3.4 nm, as verified by n&k analyzer on the monitor wafers before poly-Si deposition, and also confirmed by CV measurements. Metal antennas with various antenna area ratios (AAR) were attached to the gate. Detailed structural parameters for the devices characterized in this work are given in Table 1. After metal patterning, the remaining photoresist was stripped off in a down-stream plasma asher, which has been identified and fully characterized to be the step responsible for the observed plasma damage in our previous works [6][7]. Using the CHARM-2 sensor, we have shown that the plasma potential has a concave-shape distribution over the wafer surface, as shown in Fig.1 [6]. Such non-uniform plasma would lead to severe negative plasma charging at the wafer center, and positive plasma charging at the wafer edge.

To evaluate the device degradations due to the bias-temperature stress, the devices were subjected to stress conditions with negative gate bias (-3.5V ~ -3.9 V) and elevated temperature (100 ~ 150°C). During the stressing, drain/source and substrate were all grounded. The device parameters, including threshold voltage (V<sub>th</sub>), transconductance, and gate leakage current, were measured using an HP4145B parameter analyzer before and after the BT stressing.

### 3. Results and Discussion

Figure 2 shows the threshold voltage shift due to BT stressing as a function of stress time at different temperatures for devices with AAR of 1K. Clearly, larger shift in V<sub>th</sub> is observed at higher temperature. In addition, the NBTI is further worsened when a larger antenna is attached, as shown in Fig.3. This trend confirms the observation reported in Ref.5.

In order to understand the effects in more detail, we investigated their dependence on device location. Figure 4 shows V<sub>th</sub> of devices as a function of device location before

BT stressing. It is very interesting to find that |V<sub>th</sub>| values for devices with AAR of 60K are smaller than those of devices with AAR of 1K. This implies that more electron traps were generated in larger antenna devices during device fabrication. Nevertheless, more shift in V<sub>th</sub> after BT stressing is observed when antenna size is increased. The results are shown in Fig.5 as a function of device location. It should be noted in this figure that the V<sub>th</sub> shift is larger for devices at the wafer center and the edge, indicating that both negative (wafer center) and positive (wafer edge) plasma charging could enhance the NBTI. V<sub>th</sub> values of the devices after BT stress are shown as a function of device location in Fig.6. Contrary to the trend shown in Fig.4, the |V<sub>th</sub>| values for larger antenna devices now become comparable or even larger than those of smaller antenna devices at the same location, owing to the enhanced NBTI caused by the plasma charging (Fig.5).

### 4. Conclusions

In this study, we have clearly shown that the plasma charging could indeed enhance the NBTI of p-channel MOS transistors with ultra-thin gate oxide. One possible explanation for this is that the excess electron traps generated caused by plasma charging would increase hole trapping rate during BT stressing. However, the root cause for this phenomenon is quite complicated and more efforts are needed to fully explore the issue.

For practical manufacturing, more attention should be paid on this effect since it could severely compromise the reliability of PMOS devices. We also propose that the NBTI characterization could actually be cleverly employed as a sensitive method for characterizing the antenna effects in devices with ultra-thin gate oxide, since it has been known [8][9] that the characterization using conventional indicators is becoming more and more difficult, if not impractical, as oxide is thinned down.

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### References

- [1] C. E. Blat *et al.*, J. Appl. Phys. **69**, p.1712 (1991).
- [2] N. Kimizuka *et al.*, Symp on VLSI Technology, (1999) p.73.
- [3] R. Thewes *et al.*, Tech. Dig. of IEDM, (1999) p.81.
- [4] N. Kimizuka *et al.*, Symp on VLSI Technology, (2000) p.92.
- [5] P. E. Pagaduan *et al.*, IRPS, (2001) p.315.
- [6] H. C. Lin *et al.*, IRPS, (1998) p.311.
- [7] C. C. Chen *et al.*, IEEE EDL, **21**, p.15 (2000)
- [8] H. C. Lin *et al.*, IEEE EDL, **19**, p.66, (1998)
- [9] K. P. Cheung, P2ID, (2000) p.10.

Table 1 Structural parameters for the PMOS antenna devices.

$L_{gate}$	0.8 $\mu\text{m}$	
$W_{gate}$	5 $\mu\text{m}$	
$T_{ox}$	3.4 nm	
Gate and S/D I/I	BF <sub>2</sub> <sup>+</sup> , 5E15, 30 keV	
AAR	1K	60K
Plasma damage	small	large

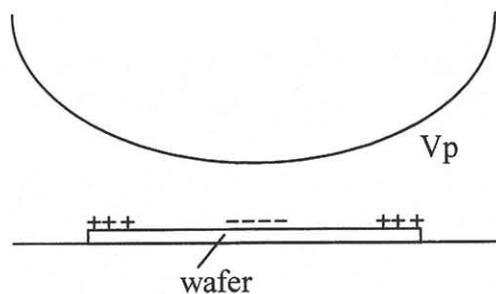


Fig.1 Plasma potential ( $V_p$ ) distribution profile in the plasma asher.

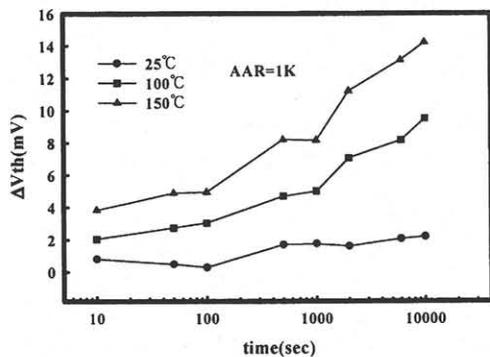


Fig.2  $V_{th}$  shift during BT stressing for PMOS devices with AAR of 1K.  $V_g = -3.5$  V.

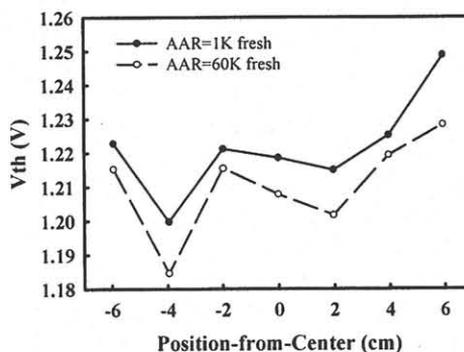


Fig.4  $V_{th}$  of PMOS devices before the BT stress as a function of the device location.

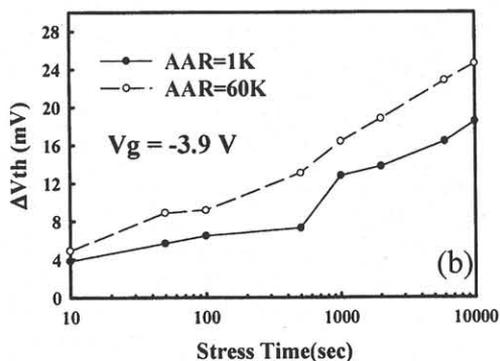
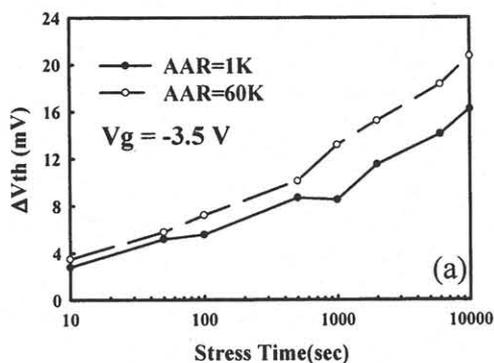


Fig.3  $V_{th}$  shift as a function of time during BT stressing at  $V_g =$  (a) -3.5 V and (b) -3.9 V. Temperature is 150 °C.

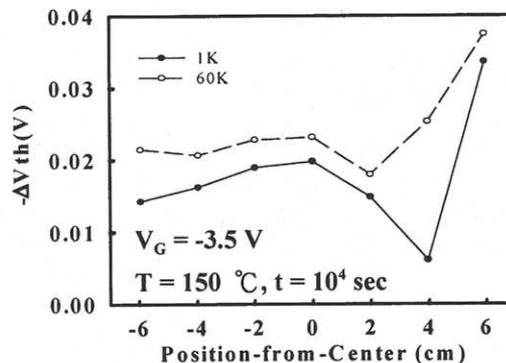


Fig.5  $V_{th}$  shift of PMOS devices after the BT stress as a function of the device location.

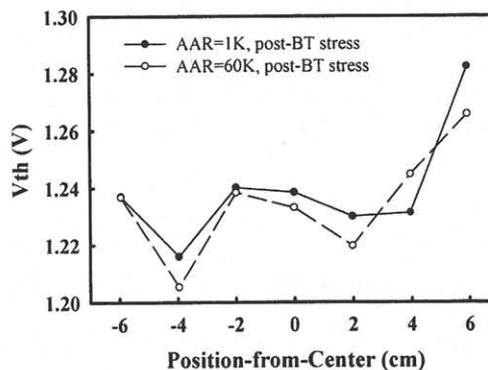


Fig.6  $V_{th}$  of PMOS devices after the BT stress as a function of the device location.