Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 208–209

B-4-3

Post-Soft-Breakdown Characteristics of Deep Sub-Micron NMOSFETs with Ultra-Thin Gate Oxide

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1. Introduction

Soft-breakdown (SBD) is frequently observed as oxide is thinned down. However, the impacts of SBD on the device characteristics of deep sub-micron NMOSFETs remain a very controversial issue. While some reports showed that its occurrence would not affect the device's switching function [1][2], some reports showed just the opposite [3]. More efforts are thus needed to address and clarify the issue.

2.Experimental

N-channel MOS transistors with n^+ poly-Si gate were fabricated on 6-inch Si wafers. Nominal gate oxide thickness and channel length/width are 2.5 nm and 0.2/10 μm, respectively. Electrical characterization was performed using a HP-4156 parameter analyzer. Some devices were stressed to breakdown under a gate bias of -4.5 V with all other terminals (i.e., source, drain, and substrate) grounded. Device characteristics before and after BD were measured and analyzed.

3. Results and Discussion

Soft breakdown events in a MOSFET could be induced at the drain/source overlap region, or at the channel region. Different BD locations may result in different effects on the device performance. Figures 1(a) ~ (d) show typical characteristics of a fresh device, BD at channel, BD at source, and BD at drain, respectively. As shown in Figs.1(b) and (c), when BD occurs at the channel or at the source, the subthreshold and on-state characteristics of are not significantly affected. In contrast, BD at the drain would dramatically increase the off-state drain current, thus degrading the switching behaviors of the device, as shown in Fig.1(d).

Although the on-current is not significantly affected when BD occurs at the channel, there are two Vg regions in the off-state (i.e., $0 \geq Vg \geq -0.7$ V and $Vg < -1.5$ V) in which Id increases from that of the fresh device (Fig.2). In the range $0 \geq Vg \geq -0.7$ V, the increase in Id is related to the stressing process, rather than the occurrence of SBD. As can be seen from Fig.3, the off-state drain current in the above Vg range increases steadily with increasing stressing time before the occurrence of SBD. In this case, the TDDB test performed on the device was interrupted several times in order to measure the Id-Vg characteristics. This Id increase could be ascribed mainly to the trap-assisted gate-induced drain leakage (GIDL)[4], since some interface traps would be generated during the constant-voltage-stress [5].

On the other hand, the increase in Id after SBD for $Vg < -1.5$ V is believed to be due to the action of the parasitic bipolar transistors formed after SBD. When BD occurs at the channel, two parasitic npn bipolar junction transistors (BJT) would be formed in the substrate, as shown in Fig.4. The two transistors share a common base (i.e., substrate) and a common emitter (i.e., n^+ poly-Si), but with separate collectors (i.e., drain and source, respectively). In this work, the action of the bipolar transistor is clearly demonstrated. One example is shown in Fig. 5. Here, only the drain-side bipolar transistor was characterized by floating the source during measurement. Figures 5(a) and (b) show Ig (or Ie) and Id (or Ic) as a function of Vdg (or Vce), respectively. The measurements were performed with the common-emitter configuration, i.e., Vg = 0. Base (substrate) current is used as the input parameter. We can see that the device is essentially operating in the saturation region when Vdg is smaller than 2 V, as evidenced by the results shown in Fig.5(c) in which Vsub is larger than both Vd and Vg. This indicates that both the emitter-base and the base-collector junctions are forward-biased. On the other hand, the device will be operating in the active mode when Vdg is larger than 2 V, so the base-collector junction becomes reverse-biased. The large offset in the Vce axis is mainly ascribed to the large parasitic emitter resistance, due to the small area of the BD spot [6]. For the current-voltage characteristics of the device with BD spot located within the channel region (Fig. 1(b) and Fig. 2), the parasitic bipolar transistors would be triggered into the active mode in the negative gate voltage region when $|Vg|$ is large enough. As a result, the drain current would be amplified, resulting in the Id increase in the highly negative Vg region, as observed.

For a BJT with an uniformly doped base, its current gain (β) is inversely proportional to the base width [7]. In Fig.4, the base widths for the drain- and source-side BJTs are approximately equal to Wd and Ws, respectively. (Note that the sum of Ws and Wd is the channel length (L)). The current gain ratio for the drain- and source-side BJTs (βd/βs) thus equals to Wd/Ws. Recently, Degraeve *et al.* [8] proposed a method for extracting the BD location in the channel. They calculated the ratio x = Id/(Id+Is) at Vg=-1.5V and Vd=Vs=0V, and showed that x is equal to Ws/L. Based on those formulas, we can deduce the following relationship:

$$\frac{\beta_d}{\beta_S} = \left(\frac{x}{1-x}\right). \qquad (1)$$

Figure 6 compares the measured data with the simulation using the above equation. Excellent agreement is achieved, indicating that the BD location indeed has important effects on the post-BD device characteristics.

4. Conclusions

It is shown in this work that the SBD location has significant impacts on deep sub-micron n-channel MOSFETs. If BD occurs at the drain, a significant leakage from the gate would destroy the normal operation of the device. For devices with BD at the channel, their switching function can be retained, however. In the latter case, a large increase in Id for Vg<-1.5V is observed, which can be ascribed to the action of parasitic BJTs formed after the occurrence of the SBD.

This work was supported by the National Science Council of R. O. C. under contract No. NSC89-2215-E317-002.

References

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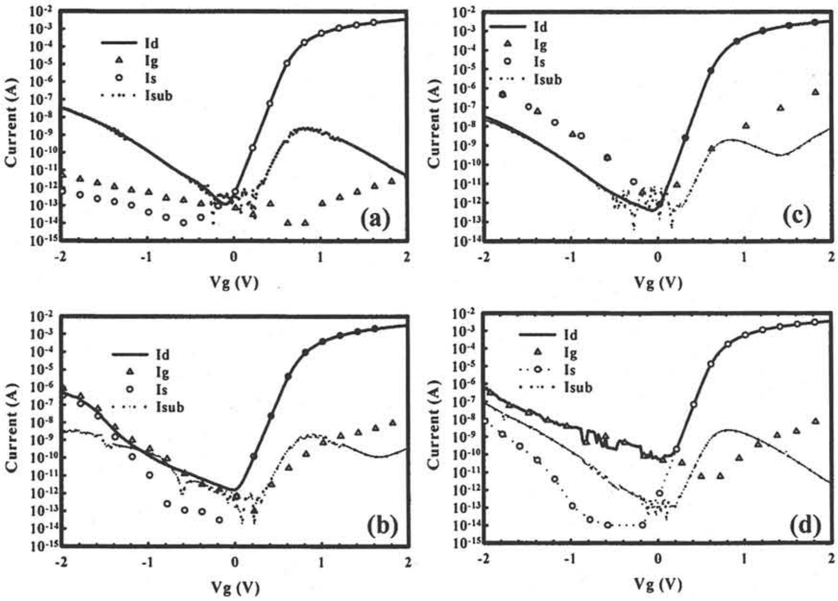


Fig.1 Current-voltage characteristics of (a) a fresh device, and first SBD incurs at the (b) channel, (c) source, and (d) drain. (Vd = 1.5 V)

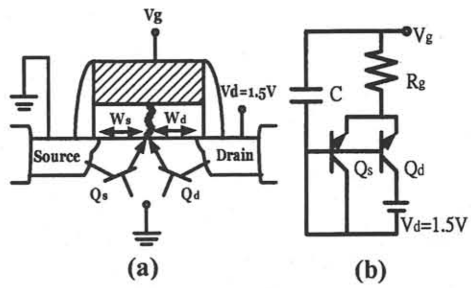


Fig.4 (a) Two parasitic BJTs would be established after BD occurs in the channel, and (b) the equivalent circuit diagram.

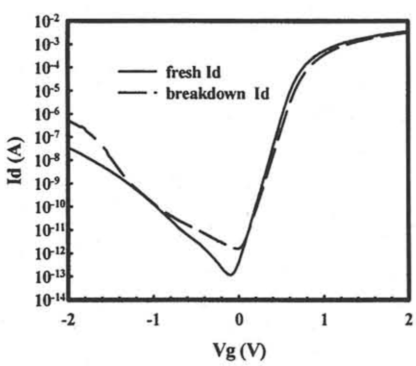


Fig.2 Id-Vg characteristics of a device before and after BD at the channel

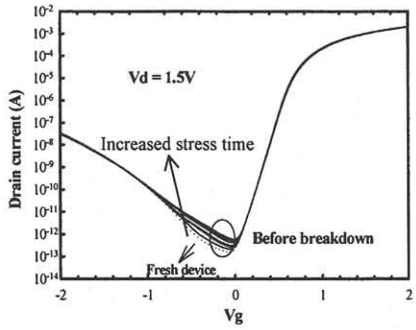
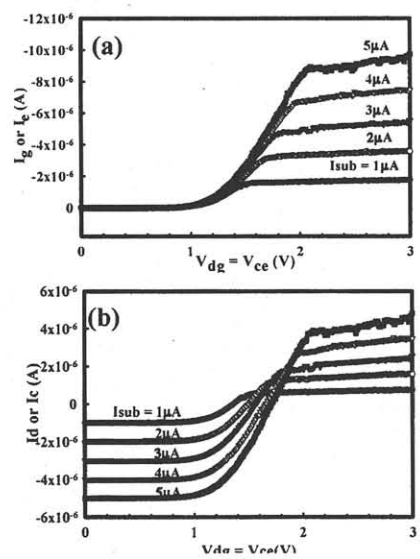


Fig.3 Id-Vg characteristics of a device with BD at the drain as a function of stressing time.



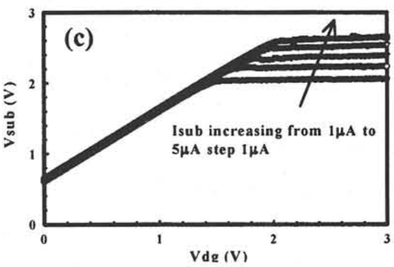


Fig.5 Characteristics of the drain-side BJT characterized with common-emitter scheme.

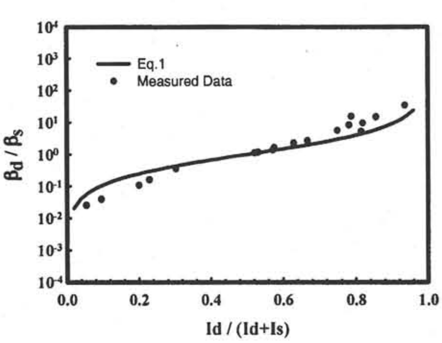


Fig.6 The post-BD parasitic BJTs' current gain ratio vs. the BD spot position.