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Current-Voltage Characteristics of Gate Oxides after Hard Breakdown

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1. Introduction

Breakdown in Metal-Oxide-Semiconductor (MOS) devices is characterized by a large conductivity increase of the gate oxide. The subsequent charge transport mechanism is of importance when considering the impact of breakdown on integrated circuits [1]. We measured current-voltage (*I-V*) curves of MOS capacitors after breakdown. The devices show diode behavior that can actually be used for substrate characterization. The measurements agree well with computer simulations.

2. Experimental details

All results were obtained on MOS capacitors with 4.5nm gate oxides and n^+ poly-Si gates. The substrates are moderately doped *p*-Si. A B^+ field implantation ($10^{11}cm^{-2}$) prevents the formation of a permanent inversion layer adjacent to the device.

To produce breakdown, a ramped current stress was applied (Fig. 1). The low gate voltage after breakdown prevents the occurrence of additional breakdown events. If the current ramp is continued to higher stress levels, fluctuations are observed. In analogy to antifuses [2], we assume that these fluctuations are due to widening of the conductive spot that is formed during breakdown. To produce different breakdown spot sizes, the ramp is terminated at different current levels I_{max}.

3. Measurement results

Figs. 2 and 3 show *I-V* curves after hard breakdown of capacitors. Breakdown results in the formation of an n^+/p junction and leads to typical diode behavior. In reverse and 'low forward' bias the current is very reproducible and scales with device size; in 'high forward' bias the current only depends on the maximum stress current I_{max}. After correction for perimeter current contributions, the reverse bias current density is typically 50pA/cm^2. In low forward bias the ideality factor is 1.03±0.01.

4. Device simulations

The program MEDICI was used to simulate the *I-V* curves after breakdown. The device structure was a circular MOS capacitor with radius r_{cap} and a gate oxide thickness of 5nm. The gate was n^+ poly-Si. The *p*-Si substrate had a thickness of 500μm and a radius of 10^4μm to account for carrier diffusion; the doping level was $10^{15}cm^{-3}$. The breakdown spot was modelled as an n^+ poly-Si cylinder with radius r_{BD}. Circular symmetry was assumed.

The simulated *I-V* curves (Figs. 4 and 5) show diode characteristics much like the measured curves. In reverse and low forward bias the current depends on the device radius r_{cap}, and in high forward bias the current varies with r_{BD}.

The r_{cap} dependence of the current is explained as follows: In reverse bias a depletion region exists under the gate. Minority carriers in this region are collected at the oxide and transported to the gate through the breakdown spot. In low forward bias, an inversion layer forms, from which minority carriers are injected into the substrate (Fig. 6). In both bias regimes, if the diffusion

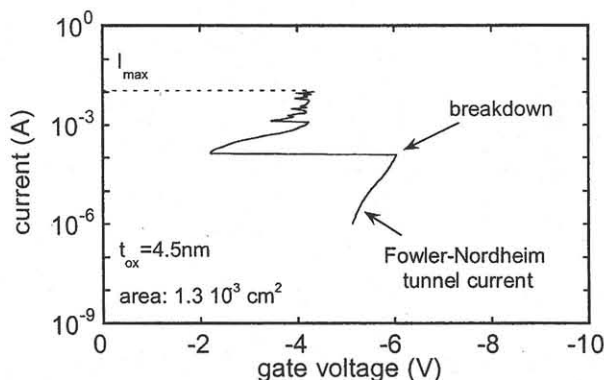

Fig. 1 – Ramped Current Stress of a MOS capacitor.

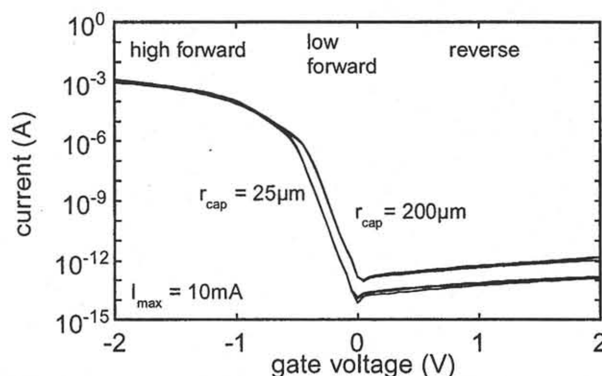

Fig. 2 – Measured *I-V* curves after breakdown on two different device areas. For each area three curves are plotted.

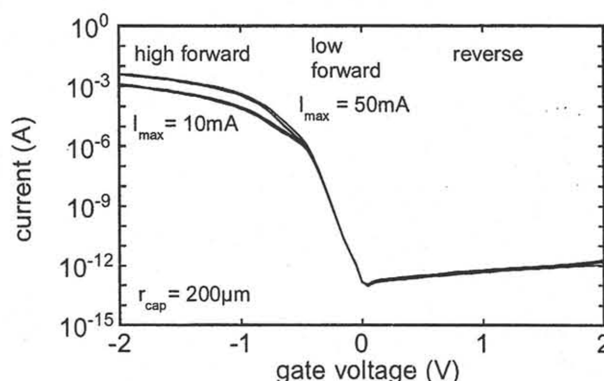

Fig. 3 – Measured *I-V* curves after breakdown for different stress levels I_{max}. For each stress level three curves are plotted.

length is much larger than r_{cap}, the current will be independent of r_{cap}. Otherwise, the current scales with device dimensions.

In high forward bias the inversion layer no longer exists, so that carriers are locally injected from the breakdown spot. This makes the current dependent on r_{BD}. Also, the barrier to majority carrier flow has vanished, and the current partly consists of majority carrier drift (high level injection).

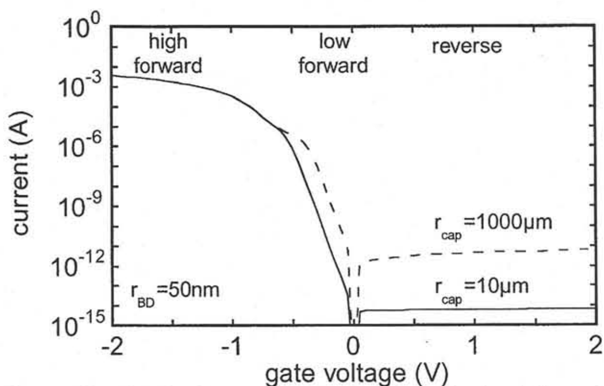

Fig. 4 – Simulated *I-V* curves of MOS capacitors after breakdown. The device radius was varied, the breakdown spot radius was kept constant.

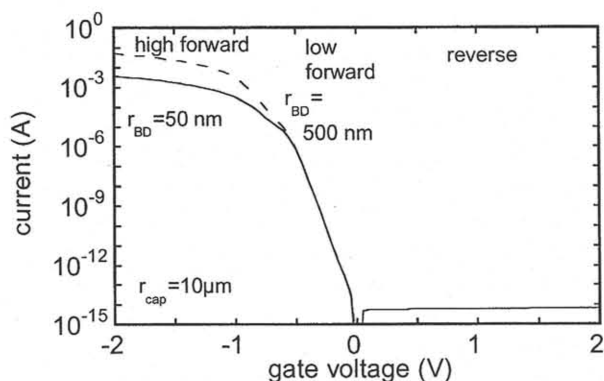

Fig. 5 – Simulated *I-V* curves of MOS capacitors after breakdown. The breakdown spot radius was varied, the device radius was kept constant.

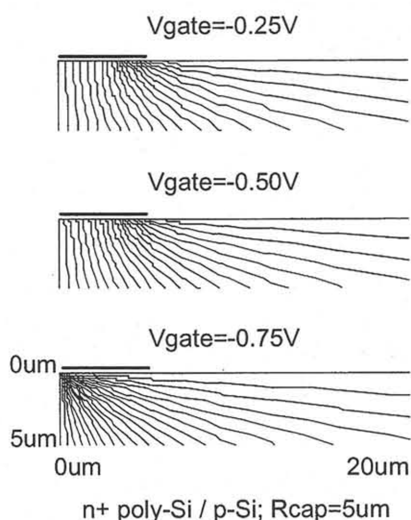

Fig. 6 – Current flowlines for a MOS capacitor after breakdown. The gate bias varies from low forward to high forward. Each pair of flowlines delineates 5% of the total current. For sake of clarity, cartesian coordinates were used in this plot.

5. Application to contaminated wafers

The diode behavior of the capacitors after breakdown suggests that they can be used for substrate characterization. To test this, wafers were deliberately contaminated with metals before gate oxidation. The metals of interest were Ti, Cu, Ni, Ru and Ca. The surface concentration was approx. 10^{12} atoms/cm^2. The defect densities in MOS capacitors were calculated from the number of early device failures in a ramped voltage test (breakdown at $|V_{gate}|<5V$). Fig. 7 shows that Ti and Ca lead to high defect densities; Ni and Cu are less detrimental and for Ru contamination the defect density is at the same level as the reference condition.

After the ramped voltage test, the diode characteristics were measured on the same devices. In reverse and low forward bias, the curves were independent of the breakdown voltage. Fig. 8 shows the reverse leakage at V_{gate}=2V. Ti, Cu, Ni and Ca contaminated wafers give results comparable to the reference condition. The Ru contaminated wafer shows a significantly higher leakage current. This result was reproduced on duplicate wafers and in different experiments. We conclude that, although Ru contamination does not lead to early failures, it affects the minority carrier lifetime in silicon. Detailed results of this contamination experiment will be published elsewhere.

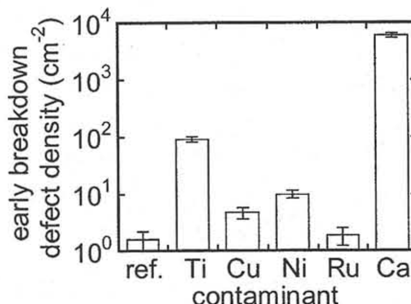

Fig. 7 – Defect densities in gate oxide as determined from ramped voltage tests. The wafers were contaminated prior to gate oxidation.

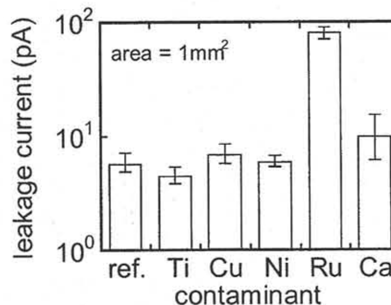

Fig. 8 – Reverse leakage currents measured on MOS capacitors after breakdown.

6. Conclusions

In MOS devices with n^+ poly-Si gate and *p*-Si substrate, gate oxide breakdown leads to formation of an n^+/p junction. In the resulting diode *I-V* curves a dependence on device dimensions was observed. Device simulations show that this is due to the presence of inversion- and depletion layers. If these are not present, the current depends on the breakdown spot size. The *I-V* curves after breakdown have been used to monitor the substrate quality on intentionally contaminated wafers. While no lifetime degradation was detected on Ti, Cu, Ni and Ca contaminated wafers, Ru contamination significantly increased the diode leakage current.

References

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