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Magnetic Tunnel Junctions and Architectures for their Use in Magnetic RAMs*

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1. Introduction

Recent advances in magnetic tunnel junctions (MTJs) have led to much higher magnetoresistance (MR) effects than had previously been demonstrated[1-2]. High MR combined with the high resistance possible in MTJs offers a uniquely attractive combination of properties for memory devices compared to all previous magnetic devices. This paper summarizes experimental progress that has been made in demonstrating tunnel junction based memories utilizing a 1-transistor/1-FET cell, and describes an alternative architecture that offers potential for higher density MRAMs.

2. The Magnetic Tunnel Junction as a Memory Element

Fig. 1a illustrates the structure of a magnetic tunnel junction. The active components of the device are two metallic ferromagnetic films and the tunnel barrier separating them. The top one of these is called the free layer and is uniaxial in nature such that it is stable when oriented either to the right or to the left. The bottom ferromagnetic film is exchange coupled to a metallic antiferromagnetic film thereby pinning the moment direction of the bottom ferromagnetic film. Finally top and bottom contact wires are illustrated for the structure. A representative stack consists of 200Cu-120IrMn-20CoFe-12Al_2O_3-10CoFe/ 40NiFe-50Ta-1000Al, where the numbers represent thicknesses in Angstroms. The device resistance response is illustrated in Fig. 1b. The moment of the top magnetic film reverses hysteretically in response to applied fields as indicated by the arrows on the diagram. At low fields the moment is stable when oriented either parallel or antiparallel to the moment of the pinned layer, the device resistance being lower when the moments are parallel. Resistance is controlled by fine adjustments of the Al_2O_3 thickness, and can range from 10 to 10^9 Ω-μm,[2] and magnetoresistance, defined as the change in resistance divided by the parallel state resistance is of order 25 to 50%[3]. Fig. 1c illustrates the stability boundary for reversing the direction of the magnetic moment. For applied x- and y- fields inside this boundary, known mathematically as an astroid curve, the moment is stable pointing to either the right or left direction. Memory write operation is possible within an array utilizing a magnetic selection method whereby combined fields from x- and y- write lines will apply a net field outside the boundary whereas x-or y-fields falling on half selected cells fall inside the astroid stability boundary.

3. The 1 MTJ-1 FET MRAM Cell Architecture

One MTJ cell configuration that has been experimentally investigated, illustrated in Fig. 2, combines an MTJ and a transistor in each cell[4-5]. In our experiments[4], the MTJ and a thin local interconnect ("Metal x" or Mx) wiring level are inserted in between the Metal 2 and Metal 3 layers of a 3 metal-layer CMOS process. Metal x connects the bottom electrode of the MTJ to a via stack down to a transistor contact in the substrate. The transistor, which has a split gate to lower on-state resistance, is used for read selection. Write selection is accomplished using x- and y- currents from the contacting Metal 3 wire and the closest adjacent Metal 2 wire.

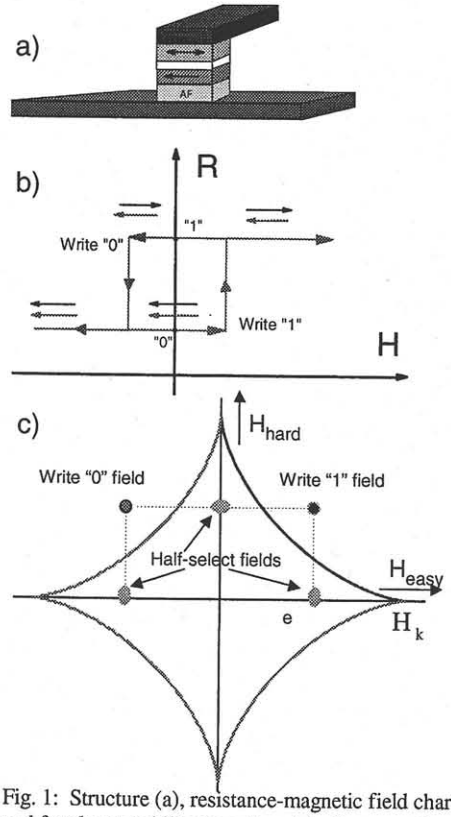

Fig. 1: Structure (a), resistance-magnetic field characteristic (b), and free layer stability boundary (c) of a magnetic tunnel junction.

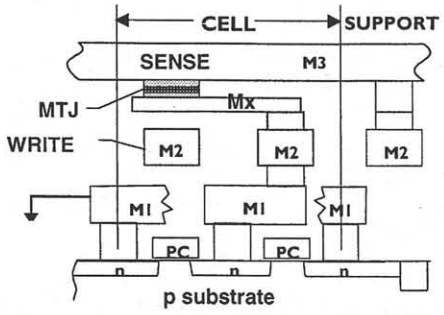

Fig. 2: 1 TJ-1 FET cell geometry

Fig. 3 gives a TEM cross-section showing three cells fabricated in 0.25 μm CMOS base technology with Al interconnect. To fabricate these samples, 200mm CMOS wafers were processed in a standard way through the via level above Metal 2. The via level was then specially thinned. The wafers were then diced into 1 inch squares, local interconnect (Mx) and magnetic tunnel junction materials were deposited, and finally the local interconnect, tunnel junction, final via level, and top interconnect (Metal 3) patterns were formed with a combination of e-beam lithography, etching, and deposition processes. Fig. 4 shows the read response obtained from address-in to data-out for yielding twin cells in a 1-kbit array fabricated on a 1mm x 1.5mm die. Separate measurements showed that a write pulse width of 2.3 ns was sufficient to reliably write cells. Cell operation was confirmed at 100 MHz, which was limited by the test system.

3. The Cross-point MRAM Cell Architecture

The FET cell architecture described in the previous section allows for fast read access times but at a cost of at least doubling the cell area due to the need to provide space for a contact to the substrate. Fig. 5 illustrates an alternative MRAM cell architecture, also enabled by the high resistance magnetic device, which does not contain the FET switch and associated via. In this "cross-point" architecture tunnel junctions are placed interconnecting each cross-point in an x- y- array of wires. Write operation in such an array is again accomplished as for the FET cell, with coincident x- and y- currents. The MTJ resistance must be high enough to prevent significant shunting of write current. The read operation is accomplished by carefully biasing one interconnection point while minimizing biasing differences across any other connection point[6]. The advantage of this cell architecture is the higher density of MTJs that can be packed into the array. A disadvantage is slower read performance, caused by the higher MTJ resistances required for avoiding shunt paths during the write operation.

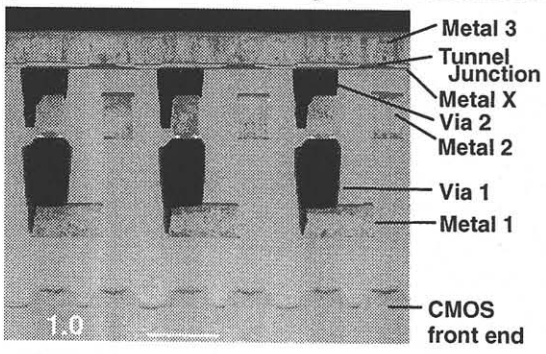

Fig. 3: TEM cross-section of three 1 TJ-1 FET cells.

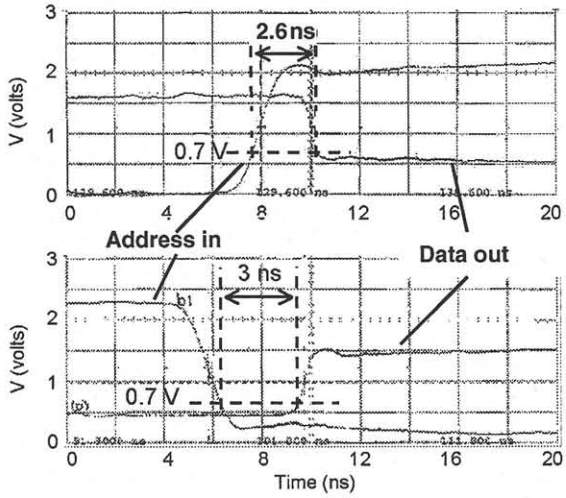

Fig. 4: Read "0" and Read "1" operations in a 1-kb FET array with the time interval from address change to data valid indicated.

4. Conclusion

The magnetic tunnel junction has been described along with its features that enable two types of MRAM architectures.

Acknowledgments

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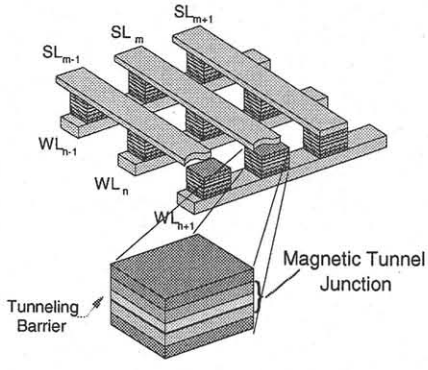

Fig. 5: Cross-point architecture