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Intrinsic Junction Leakage by Co In-Diffusion during $CoSi_2$ Formation Characterized with Damage Free n+/p Silicon Diodes

Masakatsu Tsuchiaki[1] and Kazuya Ohuchi[2]
[1] Corporate Research & Development Center, Toshiba Corporation.
[2]System LSI Research & Development Center, Toshiba Semiconductor Company
c/o 8 Shinsugita-Cho, Isogo-Ku, Yokohama, 235-8522, Japan
Phone:+81-45-770-3667 Fax:+81-45-770-3578 E-mail:masakatsu.tsuchiaki@toshiba.co.jp

1. Introduction

Based on the ITRS roadmap, the 90nm node MOSFET technology requires deep S/D junction depth, x_j, shallower than 75nm. At the same time, for sheet resistance reduction, application of silicide on the S/D is a necessity, for which, $CoSi_2$ is a prime choice. Thus, among various concerns regarding $CoSi_2$ technology, generation of junction leakage with the shallowing x_j is critical. Generally, basic researches on the $CoSi_2$ characteristics were performed mostly on bare Si wafers and analyzed commonly by physical means such as TEM[1]. On the other hand, the practical studies of the $CoSi_2$ formation were usually conducted with actual device structures and mainly examined electrically[2]. And it is widely believed that the $CoSi_2$ induced leakage is caused by some structural inhomogeneity such as silicide spikes[3]. But, for these electrical evaluations, complication may arise from possible interference of process damages incurred during device fabrication. Particularly, implantation induced end-of-range defects and dislocation loops are major concern. Also, stress build-up and associated irregularity at the STI edges could further complicate the situation. The high dose of ion implantation and the STI related issues can be avoided by forming junctions with solid phase diffusion and employing careful isolation with wet etching. Using these junctions will allow systematic examination of the $CoSi_2$ intrinsic leakage mechanism, which would then have a lasting value as a benchmark. The present paper thus reports the intrinsic $CoSi_2$ leakage using n+/p junctions formed by solid phase diffusion from AsSG. Against general expectation, these "damage-free" junctions have unveiled a substantial Co in-diffusion as a prime cause of the intrinsic leakage, which is so far not fully addressed by the practical studies.

2. Junction Formation by Solid Phase Diffusion

Fig.1 illustrates the junction formation procedure employed in this study. On 8", (100) p-type CZ wafers, B is implanted and annealed for 10min at 1190 °C to form a virtually flat p-well of $2x10^{17}cm^{-3}$ concentration over 1μm deep. The thermal process annihilates any defects associated with the implantation. After depositing a stack of TEOS and SiN films, a junction region is delineated by RIE-etching the SiN film and wet-etching the underlying TEOS film. Thus, the direct plasma damage on the substrate is avoided and some overhang of the SiN film develops (Fig.1-a). Subsequently, AsSG film is deposited and annealed to form an n+ region by solid phase diffusion into the opening defined above (Fig.1-b). As shown in the Fig. 2, As depth profiles are well described by erfc functions. Hence, by adjusting the annealing time and temperature, n+/p junctions with various depths can be readily obtained. Moreover, these junctions are free from any concerns associated with n+ implantation and residual defects. After AsSG removal by wet etching, a thin pad TEOS layer and a SiN film are applied again. Following SiN RIE stops at the pad TEOS and leaves sidewalls to stuff and guard the periphery below the overhang (Fig.1-c). For reference, junctions without the sidewall are also formed. No difference is observed between leakage with and without the sidewall. Next, on wet etching the pad TEOS, 15nm of Co, 20nm of Ti and 20nm of TiN are sequentially sputtered and the 1st RTA at 475 °C for 30s promotes 20nm CoSi formation. After removing unreacted metals, the 2nd RTA at 815 °C for 30s transforms CoSi into $CoSi_2$ about 35nm thick (Fig.1-d). Because the n+ region extends outside of the stuffing sidewall and the $CoSi_2$ formation is well contained within the n+ region, these junctions should not suffer from any anomalous leakage associated with device isolation and resultant stress. In fact, comparison of different size junctions confirmed more than 95% of leakage of a large junction (1mm x 1mm) comes from areal component. Therefore, these carefully crafted junctions provide an excellent way to characterize the intrinsic leakage properties without any major process damages.

3. Characterization of Intrinsic $CoSi_2$ Leakage

Now that the effectiveness of this test structure is confirmed, leakage generation by $CoSi_2$ formation is monitored with junctions of various depths. Fig.3 plots leakage levels (I_R at V_R=4V) as a function of the junction depth. For reference, leakage without $CoSi_2$ is also plotted. Clearly, measurable leakage generation is already in evidence at the depth of 150nm. This profile becomes even more alarming when its statistical behavior is revealed. Fig. 4 is the Weibull plot over 312 large junctions for each depth. Strikingly, generation of the leakage proceeds in each and every junction in concert. Absence of large deviation negates the presence of a sporadic and destructive leakage generator such as a silicide spike, at least in this experiment, especially for x_j below 130nm. This is further corroborated by Fig.5, which details I_R-V_R curves for each junction depth. Unlike spike-induced leakage, I-V curves shift upwards while maintaining an identical shape, i.e., the curves differ only by scaling factors. This fact and the tight ensemble distribution strongly suggest numerous formations of small leakage generators with their concentration increasing exponentially towards the Si/$CoSi_2$ interface. In fact, activation energies of the leakage currents are found to be around the mid gap, as demonstrated in Figs. 6 and 7. These facts taken together point to the generation of GR centers near the Si mid-gap. In order to further assess the nature of the GR centers, some of the junctions are additionally annealed at 800 °C. As in Fig. 8, 10min thermal process drags the leakage profile deeper into the substrate by about 15nm. Considering negligible As diffusion, involvement of some other fast diffusants is implied. Naturally, Co is the prime suspect. Indeed, direct evidence of Co involvement is brought by SIMS data measured from the backside of the substrate. As shown in Fig.9, Co seems to burst into the Si substrate mainly during transformation into $CoSi_2$. After the 2nd RTA, Co presence deep inside the substrate and its sizable inward migration by the post annealing well correlate with the post anneal leakage data. Actually, connecting the SIMS data with the leakage profile (Fig.10) allows rough estimate of the leakage per Co atom. An effective cross-section of $2.4x10^{-13}$ cm^2 comes about. This is much larger than that expected from atomic Co ($1x10^{-14}$ cm^2 [4]). With small Co solubility in Si and this large cross-section and rather slow Co movement when compared with atomic Co[4], the GR centers are thought to be some types of Co clusters or precipitates(Fig.11). Now, for the first time, a threatening character of the intrinsic $CoSi_2$ leakage has been clearly manifested.

4. Summary and Conclusion

Using solid phase diffusion, damage free n+/p junctions are fabricated to investigate an intrinsic junction leakage by $CoSi_2$ formation. With finely adjusted x_j, a first clear and systematic investigation is successfully conducted. Leakage generation by the shallowing x_j proceeds uniformly with a tight ensemble distribution. Co in-diffusion deep inside the Si substrate and resultant GR center formation are suspected as a prime cause of the intrinsic leakage. An anomalously large cross-section of the GR centers indicates Co clustering as a physical origin of the gap states. Caution is advised for the Co inward migration which could threaten the realization of future devices.

References

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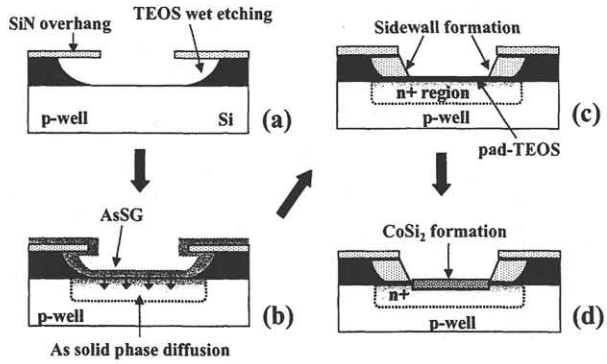


Fig. 1 n+/p junction formation procedure to fabricate damage free diodes. Solid phase diffusion from AsSG is used.

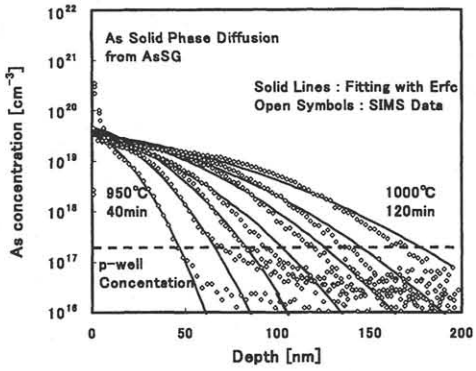


Fig. 2 As depth profiles diffused from AsSG into Si substrate by various thermal processes

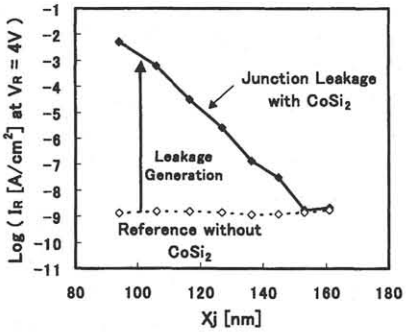


Fig. 3 Junction leakage plotted as a function of junction depth.

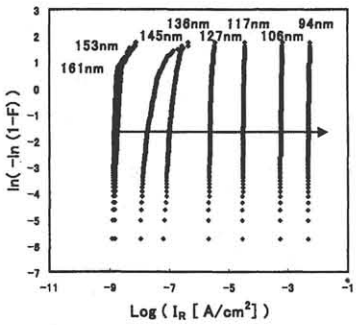


Fig. 4 Weibull plots of leakage levels over 312 junctions for various junction depths.

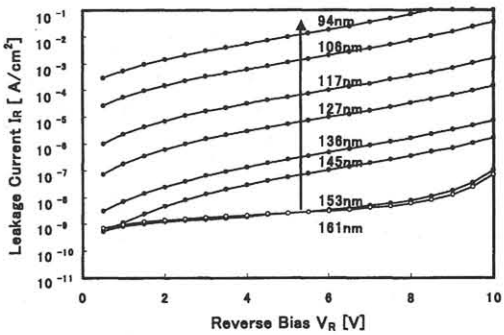


Fig. 5 Junction leakage plotted as a function of reverse bias for various junction depths.

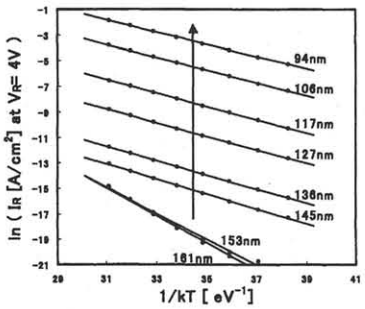


Fig. 6 Temperature dependence of leakage current for various junction depths.

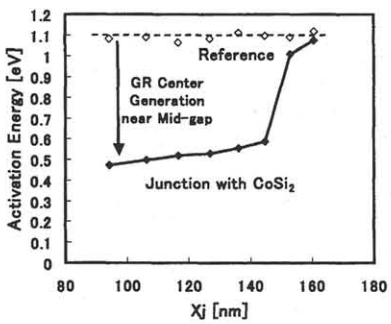


Fig. 7 Activation energies obtained from Fig.6 plotted as a function of junction depth

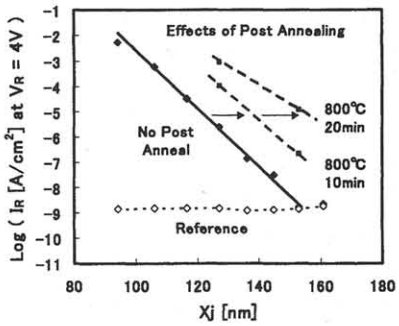


Fig. 8 Effects of post annealing on the leakage-depth profiles.

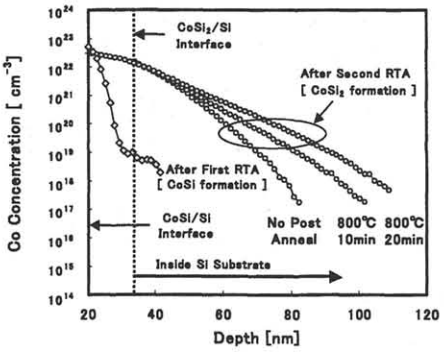


Fig. 9 Backside SIMS profiles of Co atom after RTA processes and post annealing

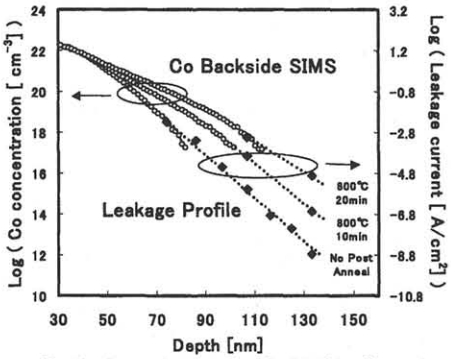
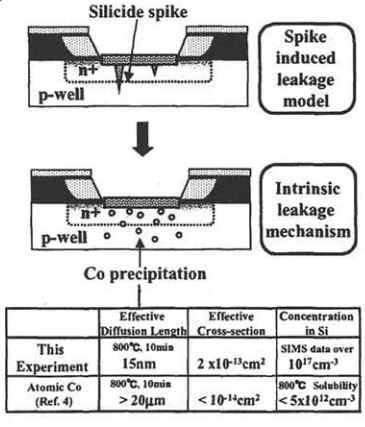


Fig.10 Comparison between Co SIMS profiles and leakage profiles. The extent of depletion layer is taken into account.



	Effective Diffusion Length	Effective Cross-section	Concentration in Si
This Experiment	800℃, 10min 15nm	2×10^{-13}cm²	SIMS data over 10^{17}cm⁻³
Atomic Co (Ref. 4)	800℃, 10min > 20μm	$< 10^{-14}$cm²	800℃ Solubility $< 5 \times 10^{12}$cm⁻³

Fig.11 Unlike widely held spike model above, Co clustering is revealed as an intrinsic leakage mechanism by this experiment