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Novel SiGe-on-Insulator Virtual Substrate Fabricated by Self-Melt-Solidification

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The strained-Si MOSFET fabricated on a SiGe virtual substrate is a promising device structure for sub-100-nm CMOS technology because of its high electron and hole mobilities. Developing this device requires a high-quality SiGe virtual substrate. The dislocation density and surface roughness of virtual substrates fabricated by present technologies, such as graded SiGe buffer-layer growth, are quite unsatisfactory; to our knowledge, the values of these parameters are at least 1×10^5 cm^{-2} and 1 nm, respectively. In this paper, we describe a novel SiGe-on-insulator virtual substrate fabricated by a self-melt-solidification technique, reducing the dislocation density and surface roughness to less than 1000 cm^{-2} and 0.5 nm, respectively.

The key concepts of this technique include the following: (1) thin SiGe layer growth on a conventional SOI wafer, (2) oxide capping on the SiGe layer, (3) annealing at a temperature in a partial-melt state to relax strain in the SiGe layer, and (4) self-solidification from the partial-melt state with Ge diffusion into the SOI layer. The liquidus-solidus curves [1] of the Si-Ge system are shown in Fig. 1. At the start of annealing, the temperature is higher than the solidus curve, as marked by "A" in the figure. During annealing at a constant temperature, the Ge content decreases due to Ge diffusion into the SOI layer, and the composition moves from "A" along the arrow and reaches point "B" below the solidus curve. We anticipated that the dislocation density could be reduced as a result of the self-melt-solidification associated with the Ge diffusion, and that the SiGe surface could remain flat as a result of the oxide capping.

The sample fabrication procedure, shown in Fig. 2, consisted of the following steps: (1) the SOI thickness of the wafer (SOITEC) was reduced to 50 nm by oxidation and wet etching; (2) a SiGe layer (100 nm) and Si cap layer (50 nm) were grown by using a solid-source MBE system; (3) the Si cap layer was oxidized at 900°C to reduce its thickness to a few nm; and (4) the sample was annealed at 1200°C for 2 h in a nitrogen atmosphere. The residual strain in the SiGe layer was estimated by Raman spectroscopy and four-crystal X-ray diffraction (XRD), depth profiles were measured by Rutherford back-scattering spectroscopy (RBS) and Auger electron spectroscopy (AES), the surface morphology was characterized by atomic-force microscopy (AFM), and the dislocation density was estimated by optical microscopic observation of a Secco-etched surface.

The Raman peak positions for samples with various Ge compositions are plotted in Fig. 3. The expansion ratio of the lattice constant of SiGe over Si (right-hand axis) was measured by XRD and is also shown. These data points lie along a dotted line obeying Vegard's rule. This clearly shows that the SiGe layers were completely strain relaxed.

The depth profiles of one sample (30% Ge) measured by RBS are shown in Fig. 4. Note that the surface oxide layer was removed. The Ge content in the SiGe layer was 32% and uniform throughout the layer (< 150 nm). The residual back-scattering ratio (χ_{min}) was 6.3%, suggesting the epitaxial nature and good crystallinity of the layer.

An AFM image of the surface of the same structure (with the oxide removed) as in Fig. 4 is shown in Fig. 5. The SiGe layer and Si cap layer of the sample were grown at room temperature and crystallized at 600°C in order to avoid roughening during the MBE growth. The surface roughness was 0.48 nm rms, which is the lowest value reported to date for a strain-relaxed SiGe virtual substrate.

Optical micrographs of the Secco-etched surfaces of (a) the same sample as in Fig. 5 and (b) a typical graded SiGe virtual substrate are shown in Fig. 6. On the graded SiGe virtual substrate, bright spots originating from threading dislocations were clearly observed. The dislocation density was estimated to be ~6×10^5 cm^{-2}. On the other hand, for the sample fabricated in the present study, there was no contrast due to crystal defects anywhere in the entire observed region (>0.01 mm^2). The dislocation density was estimated to be less than 1000 cm^{-2}.

In summary, we have developed a novel method for fabricating a SiGe-on-insulator virtual substrate by using a self-melt-solidification technique. By annealing the SiO_2-capped SiGe layer (100 nm) on an SOI wafer in a partial-melt state at 1200°C, we could achieve a uniform Ge distribution, complete strain relaxation, good crystalllinity, a smooth surface (< 0.5 nm rms), and a low dislocation density (<1000 cm^{-2}).

Acknowledgments

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References

[1] E. Kasper and K. Lyutovich (Ed.): *Properties of Silicon Germanium and SiGe: Carbon*, INSPEC, The Institution of Electrical Engineers, London UK (2000) p. 48.

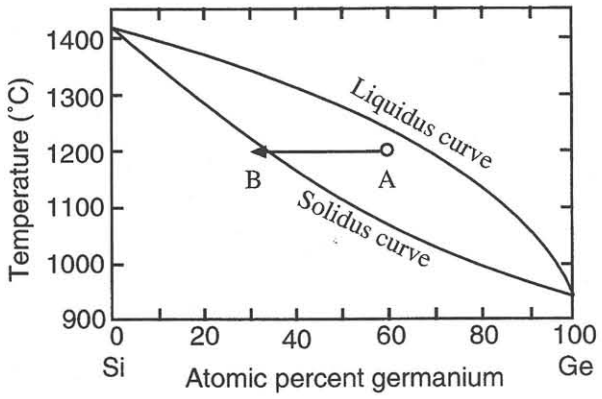

Fig. 1 Liquidus-solidus curve of the Si-Ge system

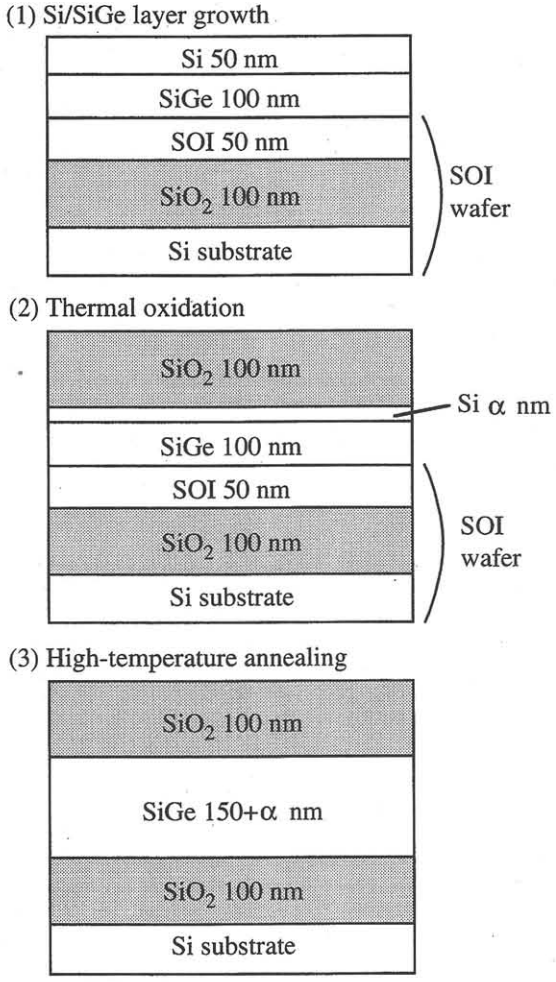

Fig. 2 Sample fabrication procedure

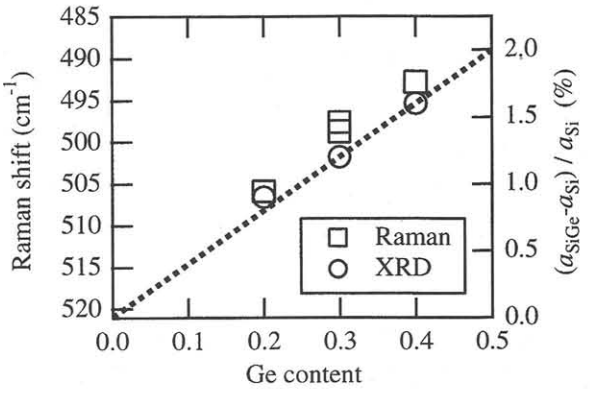

Fig. 3 Raman shift and lattice constant ratio as a function of Ge content in the SiGe layer

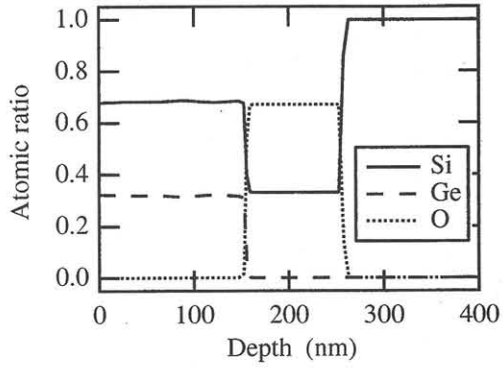

Fig. 4 Depth profiles for a 30%-Ge sample measured by RBS

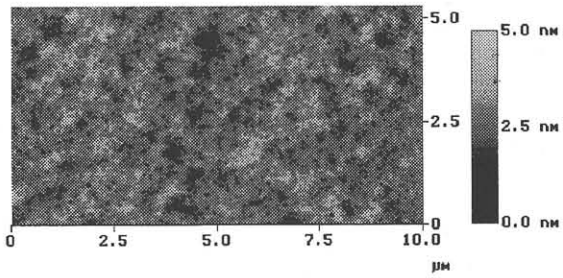

Fig. 5 AFM image of the 30%-Ge sample. The z-scale is 5 nm.

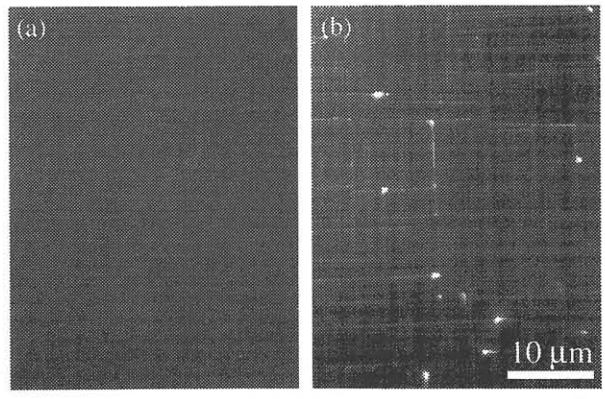

Fig. 6 Optical micrographs after defect etching for (a) the 30%-Ge sample and (b) a conventional graded SiGe virtual substrate