Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 490–491

B-8-3

Physical and Electrical Characteristics of Poly-Si/ZrO_2/SiO_2/Si MOS Structures

Kwan-Yong Lim, Dae-Gyu Park, Heung-Jae Cho, Joong-Jung Kim, Jun-Mo Yang, Il-Sang Choi, Jung-Kyu Ko, Jae-Young Kim, In-Seok Yeo, Jin Won Park, and Hee-Koo Yoon

Advanced Process Team, Memory R&D Division, Hyundai Electronics Industries Co. Ltd., Ichon P.O. Box 1010, Ichon-si, Kyoungki-do, 467-701 Korea (Phone:+82-31-630-4468, Fax:+82-31-630-4545, e-mail: kylim@sr.hynix.com)

ABSTRACT

We examine the physical and electrical characteristics of poly-Si/ZrO_2/SiO_2/p-Si metal-oxide-semiconductor (MOS) structures for the poly-Si gate compatibility with ZrO_2 gate dielectric. The MOS capacitors gated with n^+ poly-Si exhibited ideal high-frequency C-V curves up to the furnace anneal of 750℃ for 30 min with an interface trap density (D_{it}) as low as ~$5x10^{10}$ $eV^{-1}cm^{-2}$. We found several orders of magnitude lower gate leakage current from the small size (< 50x50μm^2) gate electrode pattern. Electrical and physical analyses revealed that the formation of interfacial $ZrSi_x$ nodule was responsible for the high gate leakage and was strongly dependent on the gate area and line width. Further, Boron penetration was observed from the p^+ poly-Si gated pMOS capacitors after activation anneal above 800℃.

INTRODUCTION AND EXPERIMENTAL

Most recently, ZrO_2 has been assessed for MOS device applications as an alternative gate dielectric due to the high dielectric constant (k~25) and good thermal stability with Si [1,2]. Because of critical issues such as severe thickness variation and reliability of gate oxide at the isolation edges [3], we employed ZrO_2 gate dielectric prepared by atomic layer chemical vapor deposition (ALCVD) for giga-scale CMOS devices ensuing excellent step coverage.

MOS capacitors having n^+ and p^+ poly-Si gates were fabricated on the ZrO_2/SiO_2/Si structure. The ZrO_2 films were deposited by ALCVD at ASM Microchemistry using $ZrCl_4$ and H_2O vapor at 300℃. Prior to the ZrO_2 deposition, an ultrathin (~7 Å) SiO_2 was grown for the smooth ZrO_2 nucleation [2]. The ZrO_2/SiO_2/Si stack was annealed in O_2 for dielectric improvement, followed by the preparation of poly-Si gate electrodes at 550℃, i.e., in-situ PH_3 doped n^+ poly-Si and $_{11}B^+$ implanted p^+ poly-Si. The process compatibility of poly-Si electrode with ZrO_2 gate dielectric was examined via dopant activation at 650-900℃ for 30 min in N_2.

RESULTS AND DISCUSSION

Figures 1-2 show high-frequency C-V hystereses and conductance loss (G/ω)-V curves of n^+ poly-Si/ZrO_2/SiO_2/p-Si *n*MOS capacitors as a function of activation anneal, exhibiting ideal MOS characteristics up to 750℃. The hysteresis (V_H) and interface state density (D_{it}) as determined by the $\triangle V_H$ and G/ω were reduced with anneal temperature. The $\triangle V_H$ and the D_{it} after anneal at 750℃ is ~ 10 mV and ~$5x10^{10}$ $eV^{-1}cm^{-2}$. There was slight positive shift in the flat-band voltage (V_{FB}) with anneal. This may be related with the phosphorus ($_{31}P$) diffusion into the ZrO_2/SiO_2 layer with temperature (Fig.3), which was also observed from the n^+ poly-Si/Al_2O_3/Si system [4]. However, the C-V measurements were not able to carried out for the samples annealed over 800℃ (Fig. 1). Shown in Fig 4 is J-V plots of MOS capacitors measured from the 200x200 μm^2 square electrodes. It is observed that the gate leakage current (I_{LC}) was abruptly increasing with the activation anneal above 750℃, displaying ~3 orders of magnitude higher I_{LC} (-1.5V) at 800℃ compared with the I_{LC} at 700℃. Fig. 5 depicts cross-sectional TEM images of n^+ poly-Si/ZrO_2/SiO_2/p-Si structure, showing interfacial precipitates for as-deposited and annealed samples. The size and density of those nodules are increasing with anneal temperature. The high-resolution TEM images(Fig.5) and Fourier transformed digital diffractogram (Fig.6) identified the precipitate as $ZrSi_x$, in consistent with recent report [5]. Shown in Fig. 7 are SEM images of ZrO_2 surfaces after poly-Si removal, where the $ZrSi_x$ nodules were etched out during the poly-Si removal. The size and distribution of pinholes are well matched with $ZrSi_x$ nodules, and increased with anneal temperature as well. Notably, we found a pattern-size dependent I_{LC} variation that ~ 3 orders of magnitude lower I_{LC} at −1.5V were attained even after activation anneal of 800℃-30min. This indicates that the presence and/or density of interfacial $ZrSi_x$ nodule may be rare on the smaller pattern size (< 50x50μm^2) due to the limited silicidation reaction at the narrow gate area and line width (Fig. 8).

The cumulative I_{LC} distribution of p^+ poly-Si gated pMOS capacitors (200x200 μm^2) and pattern-size dependent I_{LC} characteristics were plotted with anneal in Figs 9-10. The smaller size (< 50x50μm^2) capacitors exhibited ~4 orders of magnitude lower I_{LC} than the large size capacitors. However, the capacitors annealed at 900℃ showed very leaky I_{LC} characteristics regardless of pattern size, resulting in the incompatible poly-Si gate with ZrO_2 at 900℃. Figs.11-12 displayed C-V and SIMS profiles of p^+ poly-Si gated pMOS capacitors. The V_{FB} shifts of +0.18V with the anneal from 800 to 850℃ and +0.2V from 850℃ to 900℃ were observed due to the boron penetration, although the C-V data from 900℃ was too leaky to compare each other (Fig. 11). The boron profiles in p^+ poly-Si/ZrO_2/SiO_2/n-Si structure (Fig.12) confirmed the conspicuous boron penetration responsible for the noted $\triangle V_{FB}$ in Fig.11. The diffusion path of B can be the grain boundaries of polycrystalline ZrO_2 or $ZrSi_x$ at the elevated temperatures.

In summary, we attained ideal C-V characteristics from the n^+ poly-Si gated nMOS capacitors up to 750℃ with the D_{it} of ~$5x10^{10}$ $eV^{-1}cm^{-2}$, whereas boron penetration was observed from the p^+ poly-Si gated pMOS capacitors after activation anneal over 800℃. While several orders of lower I_{LC} was obtained from small-size capacitors, the formation of interfacial $ZrSi_x$ nodules at 900℃ was hardly capable of prohibiting even at 0.8μm-wide gate line.

REFERENCES

[1] W.-J. Qi *et al.*, *IEDM Tech. Dig.*, p.145 (1999).
[2] M Copel *et al.*, *Appl. Phys. Lett. 76*, p.436 (2000).
[3] C.T. Liu *et al.*, *VLSI Tech. Dig.*, p.75 (1999).
[4] J.H. Lee *et al.*, *IEDM Tech. Dig.*, p.645 (2000).
[5]C. Hobbs *et al. Int. Symp. on VLSI-TSA*, p.204 (2001).

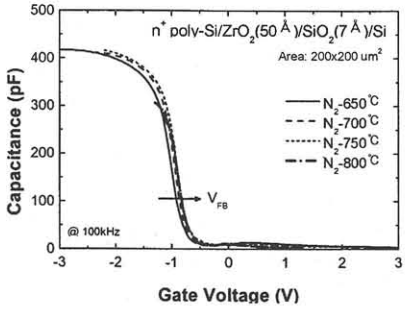

Fig.1. C-V hysteresis curves of the n+ poly-Si/ZrO_2(50 Å)/SiO_2(7 Å)/p-Si nMOS capacitors.

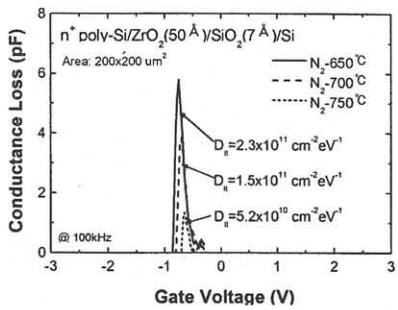

Fig.2. Conductance loss (G/ω)-V curves of the n+ poly-Si/ZrO_2(50 Å)/SiO_2(7 Å)/p-Si nMOS capacitors.

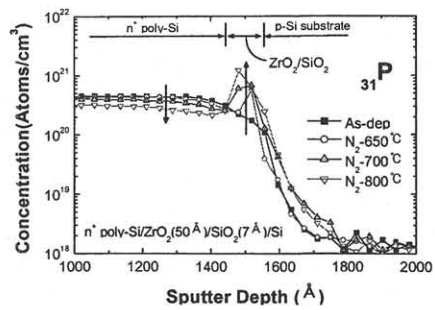

Fig.3. Phosphorus profiles in the n+ poly-Si/ZrO_2(50 Å)/SiO_2(7 Å)/p-Si as a function of activation anneal.

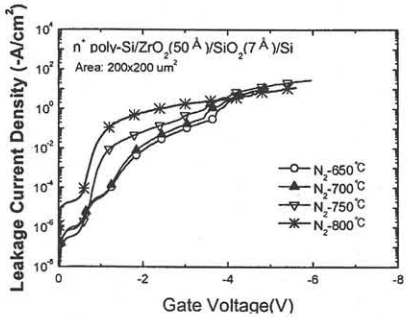

Fig.4. I-V characteristics of the n+ poly-Si/ZrO_2(50 Å)/SiO_2(7 Å)/p-Si nMOS capacitors as a function of activation temperature.

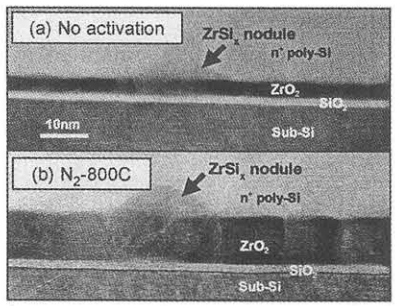

Fig. 5. Cross-sectional TEM images of n+ poly-Si/ZrO_2/SiO_2(7 Å)/p-Si nMOS capacitors: (a) no activation for ZrO_2 50 Å and (b) N_2-800C-30m for ZrO_2 140 Å.

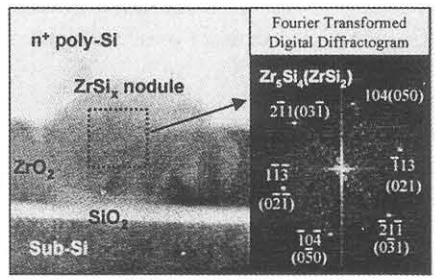

Fig. 6. XTEM images of n+ poly-Si/ZrO_2/SiO_2(7 Å)/p-Si with 800C anneal in N_2 (left) and its Fourier transformed digital diffractogram image (right): the structure of $ZrSi_x$ nodule is expected to be Zr_5Si_4(tetragonal: PDF #72-2097) or $ZrSi_2$ (orthorhomic: PDF #74-1053).

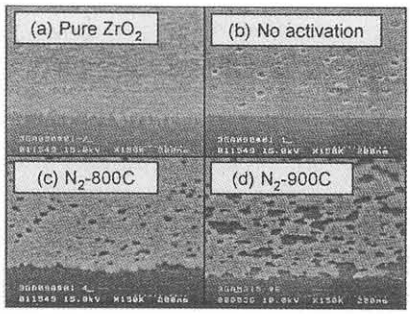

Fig. 7. SEM images of ZrO_2 surfaces as a function of activation temperature: (a) as-deposited ZrO_2, (b) no activation, (c) 800℃, and (d) 900℃ in N_2-ambient for 30min. The surface morphologies of ZrO_2/SiO_2/Si were examined after poly-Si removal.

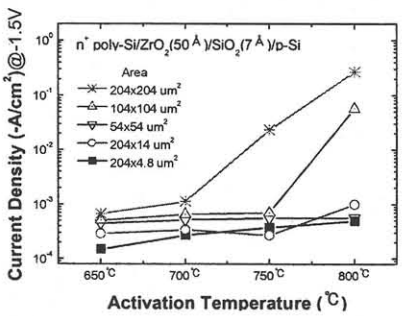

Fig. 8. Pattern-size dependency of leakage currents of the n+ poly-Si/ ZrO_2(50 Å) /SiO_2(7 Å)/p-Si: plotted as a function of activation anneal.

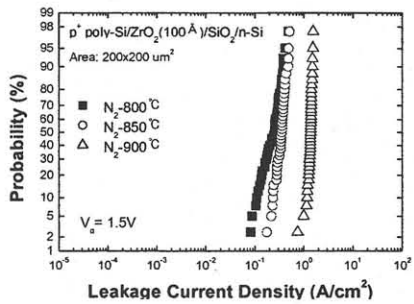

Fig. 9. Cumulative probability of leakage currents of p+ poly-Si/ZrO_2(100 Å)/SiO_2(7 Å)/n-Si pMOS capacitors: measured at V_g=1.5V.

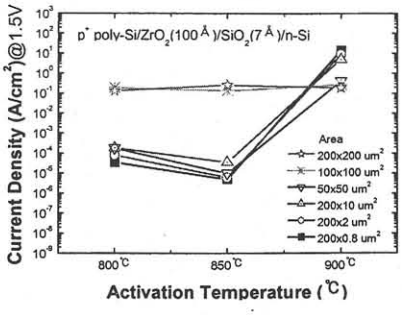

Fig. 10. Pattern-size dependency of leakage currents of the p+ poly-Si/ZrO_2(100 Å)/ SiO_2(7 Å)/n-Si : plotted as a function of activation anneal.

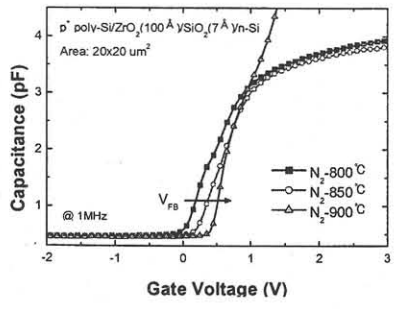

Fig. 11. C-V curves of the p+ poly-Si/ ZrO_2(100 Å)/SiO_2(7 Å)/n-Si pMOS capacitors.

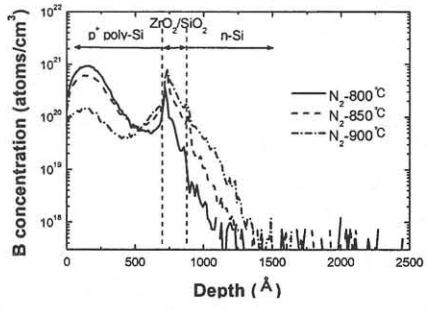

Fig. 12. Boron profiles in the p+ poly-Si/ZrO_2/SiO_2/n-Si as a function of activation anneal.