Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 496–497

B-9-1

Low Leakage La_2O_3 Gate Insulator Film with EOTs of 0.8–1.2 nm

S. Ohmi, C. Kobayashi, E. Tokumitsu, H. Ishiwara and H. Iwai
Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama, 226-8502, Japan
Phone: +81-45-924-5471, Fax: +81-45-924-5487, E-mail: ohmi@ae.titech.ac.jp

1. Introduction

Among the high-k dielectric materials, ZrO_2 and HfO_2 are popularly studied for next generation gate insulator because of their relatively high dielectric constant value (20 –30) and relatively high stability at the Si interface. However, in most of the cases, interfacial layer formation during the heat process and insufficient quality of the deposited film makes it difficult to obtain small equivalent oxide thickness (EOT) with low gate leakage current. Currently, the smallest EOT value with considerably small gate leakage current was realized by La_2O_3 film [1] rather than ZrO_2 or HfO_2 films. However, there have been no reports since then about La_2O_3 films, which confirmed this excellent results. Even, some worse results for La_2O_3 were reported after that [2].

Purpose of this paper is to confirm if La_2O_3 film can realize small EOT value with low leakage, and also to study some optimum process conditions for the film.

2. Experimental

Figures 1(a) and (b) show La_2O_3 thin film deposition method for the literature [1] and our case, respectively. In the case of the literature, thin La metal film was first deposited on p-type Si substrate by MBE and then the La film was selectively oxidized at low temperature below 400°C to form amorphous La_2O_3 as shown in Fig. 1(a). In our case, amorphous La_2O_3 film itself was deposited on n-type Si by using an MBE equipment as shown in Fig. 1(b). Some details of the process are described below.

La_2O_3 thin films (Physical film thickness, T_{phys}: 8 nm) were deposited on n-Si(100) substrates by molecular beam deposition (MBD). In this work, a La_2O_3 source was used for electron beam evaporations. The La_2O_3 films were deposited at R.T.-400°C. The deposited films were subsequently annealed by rapid thermal annealing (RTA) at 400-600°C in O_2 or N_2 for 5 min. Then, aluminum gate electrodes (ϕ110 μm) were formed by evaporation. C-V, J-V, AFM and cross-sectional TEM measurements were carried out to characterize these films.

3. Results and Discussion

Figure 2 shows the typical AFM images deposited at R.T. and 250°C. It was found that the surface morphology was significantly improved by deposition at higher temperature. Figure 3 shows a cross-sectional TEM image for La_2O_3/n-Si deposited at 250°C followed by 600°C O_2 RTA. It was found that extremely smooth interface was realized at 250°C deposition.

Figure 4 shows typical high-frequency C-V and J-V characteristics for La_2O_3 MOS capacitors. At 250°C deposition, as-deposited EOT value of 0.84 nm was obtained with a leakage current of 1 A/cm^2 at +1 V. By annealing the film at O_2 600°C, the leakage current was dramatically reduced to 1.7 x 10^{-8} A/cm^2 as shown in Fig. 4(b), while the EOT increased to 1.26 nm and hysteresis of the C-V curve disappeared as shown in Fig. 4(a). This is assumed to be due to the annihilation of the oxygen vacancies as well as the growth of a thin interfacial layer during RTA.

Figure 5 shows typical C-V and J-V curves for different process conditions. With 250°C deposition, N_2 400°C anneal suppressed the oxidation (even N_2, it was slightly oxidized by residual O_2 or H_2O), and EOT value increase was suppressed, but the J-V current reduction was also suppressed. With 400°C deposition, EOT of 0.88 nm with leakage current of 5.5 x 10^{-4} A/cm^2 was realized.

Figure 6 compares our EOT vs. leakage current data with the reported results for various high-k materials. Although the leakage current increases with decrease in EOT, our data are on the lowest line except the one reference point of La_2O_3 on p-Si published by [1]. Please note that filled symbols represent the results of n-Si substrate with +1 V at the gate electrode, and this is more severe condition than p-Si case represented with open symbols. It can be said now, that, together with the reference point, La_2O_3 gives so far the best EOT vs. leakage current relation among various high-k candidates.

4. Conclusions

Amorphous La_2O_3 thin films deposited on n-Si(100) by e-beam evaporation using La_2O_3 source were investigated. EOTs of 0.8-1.2 nm were realized for the films deposited at 250-400°C with the lowest leakage current densities. The uniformity of the film was the same order to thermal SiO_2.

In conclusion, La_2O_3 seems to be a strong candidate for next generation high-k gate insulator.

Acknowledgments

This work was partially supported by Semiconductor Technology Academic Research Center (STARC). The authors would like to express sincere thanks to Dr. T. Chikyow for useful discussion in evaluation of the film. The authors also would like to thank Ms. K. Nakajima for the technical support in TEM observations.

References

[1] A. Chin et al., *Symp. on VLSI Tech. Dig.*, 16 (2000).
[2] A. Kingon et al., *Ext. Abst. SSDM*, 226 (2000).

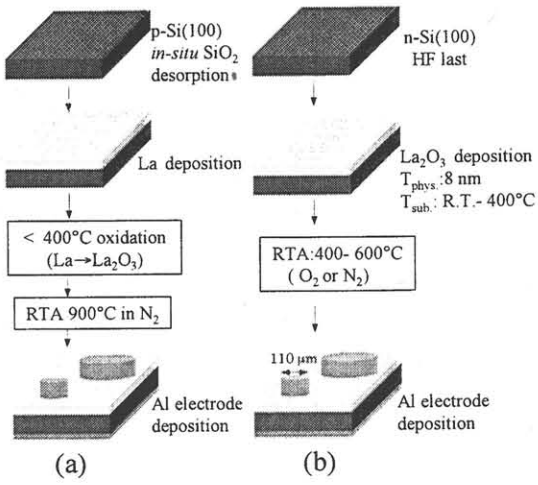

Fig. 1 $Al/La_2O_3/Si(100)$ capacitor fabrication process. (a) Reported method [1] and (b) our method.

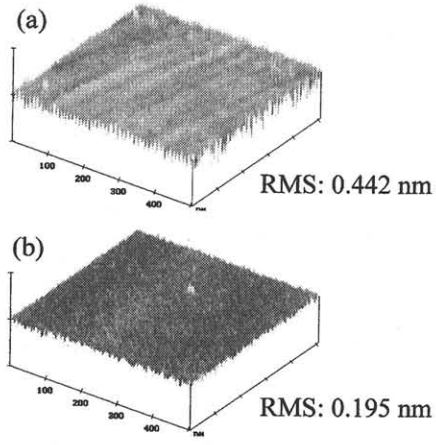

Fig. 2 Typical AFM images for La_2O_3/n-Si(100) deposited at (a) R.T. and (b) 250°C (0.5 μm x 0.5 μm, z: 5 nm/div).

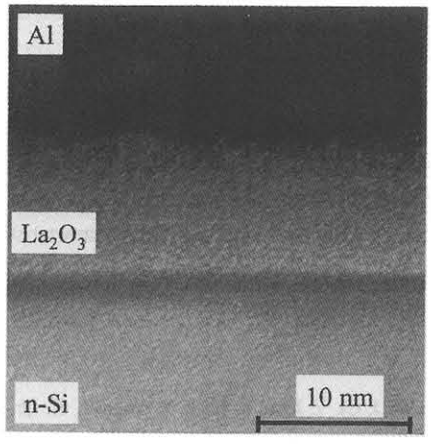

Fig. 3 Cross-sectional TEM image for La_2O_3/n-Si(100) deposited at 250°C and annealed at 600°C in O_2.

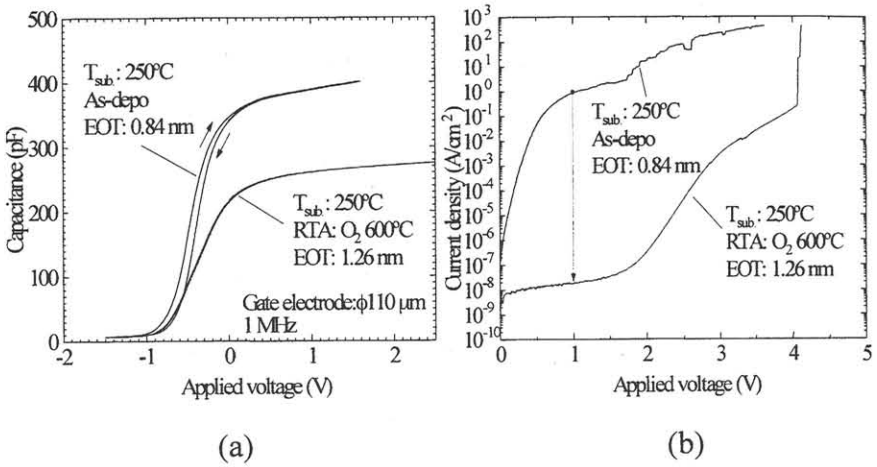

Fig. 4 Typical C-V and J-V characteristics for La_2O_3/n-Si(100) deposited at 250°C. (a) C-V and (b) J-V.

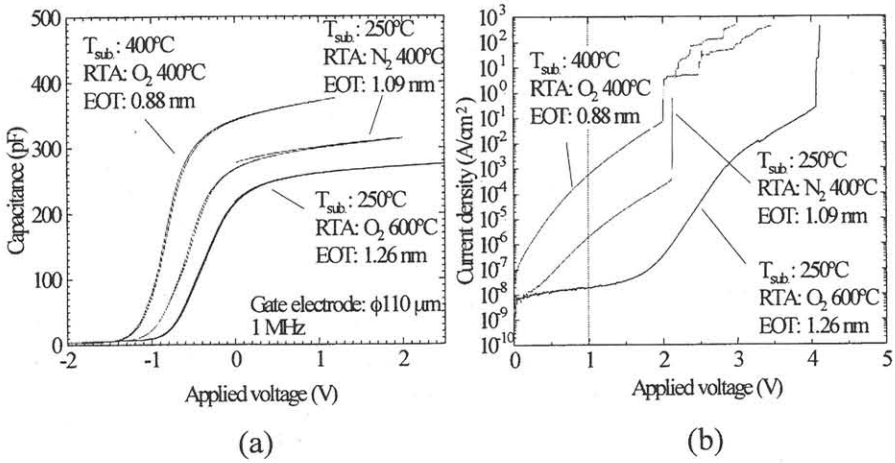

Fig. 5 Typical C-V and J-V characteristics for La_2O_3/n-Si(100). (a) C-V and (b) J-V.

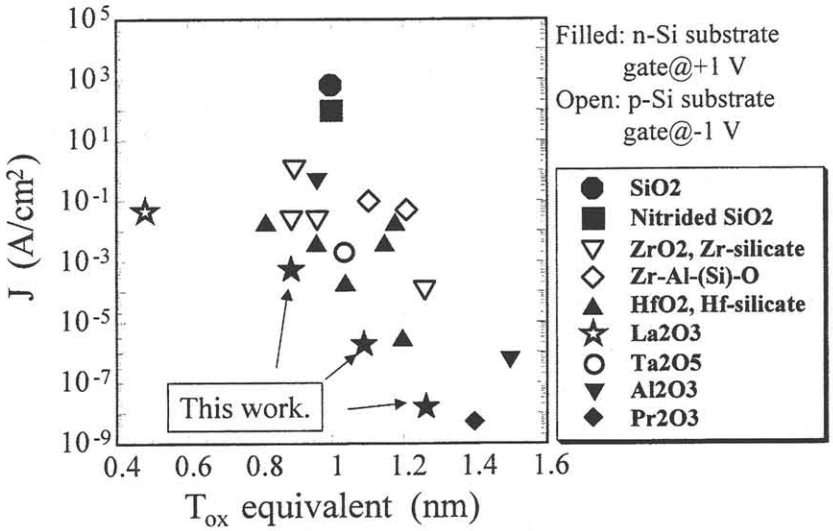

Fig. 6 Reported leakage current densities for various high-k materials.