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PVD Tantalum Oxide with Buffer Silicon Nitride Stacked High-k MIS Structure Using Low Temperature and High Density Plasma Processing

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1. Introduction

Recently, next generation gate dielectric candidates such as HfO_2[1], La_2O_3[2], and Pr_2O_3[3] etc. are studied and examined in many laboratories. Every foregoing materials have higher dielectric constant than conventional Si-based materials. However high-k gate dielectric structure must satisfies many other requirements such as higher barrier hight for careers, higher thermal stability, and lower interface trap density. Moreover, low temperature processing[4] is the additional requirement because metal substrate structure[5] and shallow and precise dopant profile require low temperature processing. In this paper, we describe high-k MIS structure formation technology using low temperature and high density plasma processing.

2. Experimental

Tantalum nitride / tantalum oxide / silicon nitride / silicon MISTD and FD-SOI MISFET were fabricated and examined. 8~12 Ω·cm (100) n-type Si wafer or SOI wafer (10 Ω·cm (100) p-type ELTRAN T_{SOI}=48nm) were adopted in this purpose. Figure 1, 2 shows process flow of MISTD, FD-SOIMISFET, respectively. Interfacial buffer Si_3N_4 layer was formed using high density microwave excited Ar/NH_3 plasma[6]. Tantalum oxide films were formed by reactive sputtering from tantalum oxide target in Kr/O_2 mixed plasma. Tantalum nitride gate electrode was formed by reactive sputtering using Xe/N_2 mixed plasma[7]. Every processes forming these MIS structure were executed below 500°C.

3. Results and Discussion

Figure 3 exhibits leak current property of TaO_X/Si_3N_4 MISTD with different TaO_X deposition method. Case (a) reveals TaO_X layer made by sputtering from Ta target subsequent Kr/O_2 plasma annealing. Case (b) shows TaO_X layer fabricated by sputtering from Ta_2O_5 target. Case (b) shows lower leak current even the same EOT thickness as case (a). This is because TaO_X layer formed from Ta_2O_5 target contains less oxide defect than that made from Ta target. Therefore to form strong TaO_X dielectrics, Adoption of Ta_2O_5 target is desirable.

Figure 4 shows J-V characteristics of TaO_X/Si_3N_4 MISTD with Al electrode on gate dielectric layer. After forming gas anneal, leak current density rises because of diffusion of Oxygen atoms to Al electrode from TaO_X layer. Oxide defects in TaO_X film degrade leak current property.

Otherwise, Fig. 5 shows J-V characteristics of MISTD with TaN_X electrode. In case of TaN_X electrode, there is no increase of leak current after forming gas anneal. This fact exhibits TaN_X/TaO_X interface has large thermal stability than Al/ TaO_X and suitable for high-k MIS structure.

Figure 6 mentions crystalline structure of TaO_X films. Figure 6 shows the XRD spectrum and TEM micrograph of TaO_X films formed in several methods. Sample conditions are (1) as deposit (400°C), (2) after Kr/O_2 plasma post-annealing (400°C), and (3) after O_2 furnace anneal (800°C) respectively. After 800°C anneal, TaO_X films exhibits poly-crystalline structure. It is not desirable because poly-crystalline gate dielectric may permit large leak current through its grain boundary. However after Kr/O_2 plasma anneal (400°C), TaO_X layer remains amorphous. Figure 6 also shows TEM analysis of as deposited TaO_X films. No bright spot can be seen. Therefore TaO_X films discussed in this paper are amorphous and suitable for thin gate dielectrics.

Figure 7 shows high frequency C-V characteristics of $TaN_X/TaO_X/Si_3N_4$ MISTD. The histeresis of C-V curve is less than 40mV and the shape of C-V curve seems to be fine.

Figure 8 shows relationship between TaO_X physical thickness and EOT thickness of TaO_X/Si_3N_4 MISTD. All samples has Si_3N_4 buffer layer in the same thickness (1.3nm (physical)). Blank square represents MISTD without Si_3N_4 buffer layer. With the same TaO_X thickness, MISTD with Si_3N_4 buffer layer shows thinner EOT value. This means Si_3N_4 buffer layer works as an anti-oxidation layer of Si substrate. An intercept value (EOT=1.47nm) reveals interfacial layer EOT thickness between TaO_X layer and Si substrate. This value is larger compared with Si_3N_4 layer thickness (1.3nm (physical)). This means Si_3N_4 layer was partly oxided during TaO_X layer deposition. This fact can be disadvantage to form ultra thin EOT gate dielectric structure. We think this partial oxidation is avoided by optimizing of sputtering conditions. The slope of the straight line in Fig.8 reveals dielectric constant of TaO_X layer. Calculated dielectric constant value is 22.6. This value is comparable with that of ideal Ta_2O_5 in spite of low temperature processing and amorphous structure.

Figure 9 shows relationship between EOT of $TaN_X/TaO_X/Si_3N_4/Si$ MISTD and leak current density at 1V stress. TaO_X/Si_3N_4 dielectric in this work exhibits lower leak current than Si_3N_4 dielectric in the thin film region.

Figure 10 and 11 exhibit V_g-I_d and V_d-I_d characteristics of n-channel FD-SOI MISFET having $TaN_X/Ta/TaN_X/TaO_X/Si_3N_4/Si$ structure, respectively. Physical thickness of TaO_X and Si_3N_4 layer are 5.8nm and 2.3nm, respectively and EOT thickness of TaO_X/Si_3N_4 is 2.98nm. Measured subthreshold slope is 66.9 mV/dec. Figure 11 represents accurate operation of this MISFET. Interface trap density (D_{it}) calculated with actual and ideal subthreshold slope is 4.29×10^{11}/eV/cm^2.

4. Conclusion

$TaN_X/TaO_X/Si_3N_4/Si$ MISTD and $TaN_X/Ta/TaN_X/TaO_X/Si_3N_4/Si$ FD-SOI MISFET are fabricated in low temperature with high density plasma processing. 1.82nm (EOT) MISTD exhibits low leak current of 6×10^{-4} A/cm^2 at 1V stress. FD-MISFET using TaO_X/Si_3N_4 works correctly.

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References

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1: Isolation (Field Oxidation)
2: Si_3N_4 buffer layer formation
~Ar/NH_3 Microwave-excited (2.45GHz) Plasma Direct Nitridation **(500°C)**
3: TaO_X layer formation
~RF Sputtering - Ta_2O_5 Target & Kr/O_2 Plasma (13.56MHz) **(400°C)**
4: TaN_X gate electrode formation
~RF Sputtering - Ta Target & Xe/N_2 Plasma (40.68MHz)
5: Al evaporation & pad electrode patterning
6: Forming gas anneal - N_2/H_2 **(400°C)**

Fig.1 Process flow of $TaN_X/TaO_X/SI_3N_4/Si$ structure MISTD. After isolation, all processes were executed below 500°C.

[5] A. Morimoto et al., SSDM, p.418 (2000)
[6] K. Sekine et al., IEEE T-ED, vol.47, No.7, p.1370 (2000)
[7] H. Shimada et al., SSDM, p.460 (2000)

1: Mesa isolation
2: TaO_X/Si_3N_4 layer formation
~Ar/NH_3 Microwave-excited (2.45GHz) Plasma Direct Nitridation **(500°C)**
~RF Sputtering - Ta_2O_5 Target & Kr/O_2 Plasma (13.56MHz) **(400°C)**
3: $TaN_X/Ta/TaN_X$ gate electrode formation
~RF Sputtering - Ta Target & $Xe/(N_2)$Plasma (40.68MHz)
4: S/D ion implantation ~$^{75}As^+$ 1.5×10^{15} 15keV
5: S/D activation anneal **(450°C)**
6: Metallization **(<400°C)**
7: Forming gas anneal - N_2/H_2 **(400°C)**

Fig.2 Process flow of $TaN_X/Ta/TaN_X/TaO_X/Si_3N_4/Si$ structure FD-SOI MISFET. Though whole processes, process temperature was below 500°C.

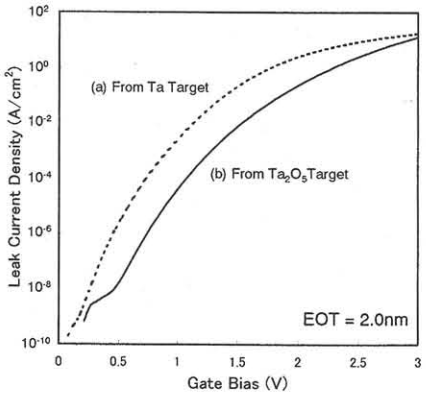

Fig.3 Leak current density difference using (a) Ta or (b) Ta_2O_5 target. Flat-band voltage equals gate bias=0.

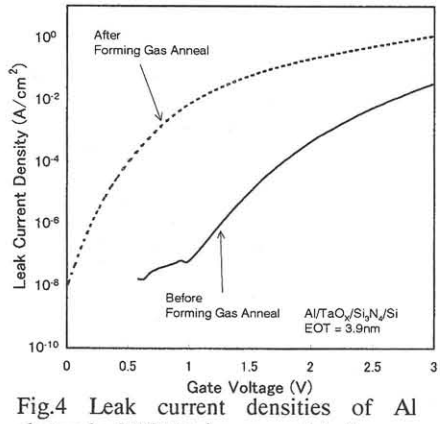

Fig.4 Leak current densities of Al electrode MISTD in case of before or after forming gas anneal. Flat-band voltage equals gate bias=0.

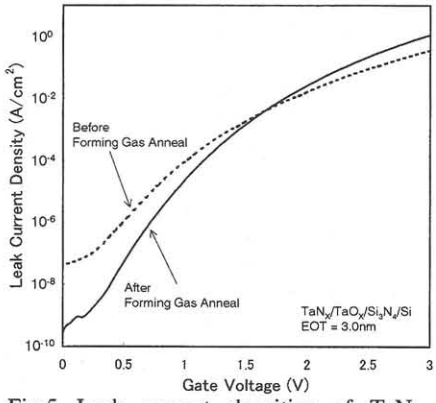

Fig.5 Leak current densities of TaN_X electrode MISTD in case of before or after forming gas anneal. Flat-band voltage equals gate bias=0.

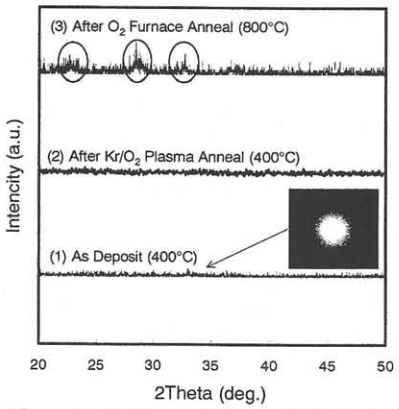

Fig.6 Crystalline property of TaO_X films. XRD and TEM analysis were executed.

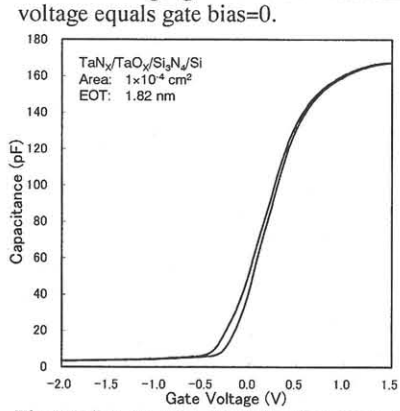

Fig.7 High frequency C-V characteristic of $TaN_X/TaO_X/SI_3N_4/Si$ structure MISTD (EOT=1.82nm).

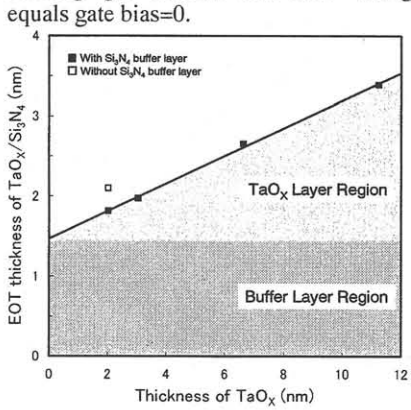

Fig.8 Relationship between TaO_X thickness and TaO_X/Si_3N_4 EOT.

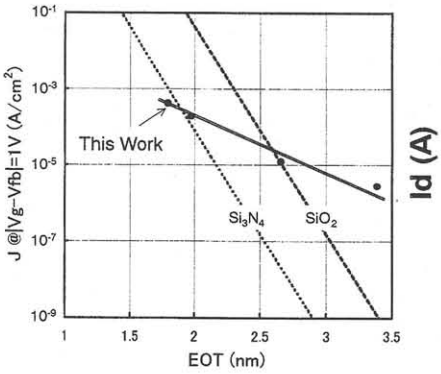

Fig.9 Relationship between EOT and leak current density of TaO_X/Si_3N_4 MISTD.

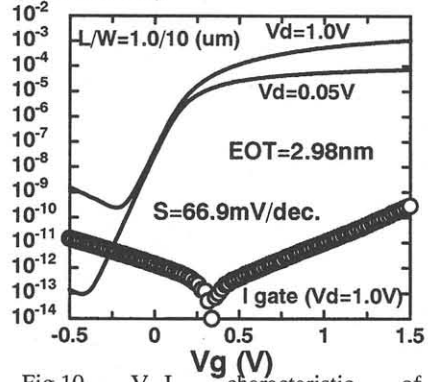

Fig.10 V_g-I_d characteristic of $TaN_X/Ta/TaN_X/TaO_X/Si_3N_4/Si$ structure FD-SOI MISFET.

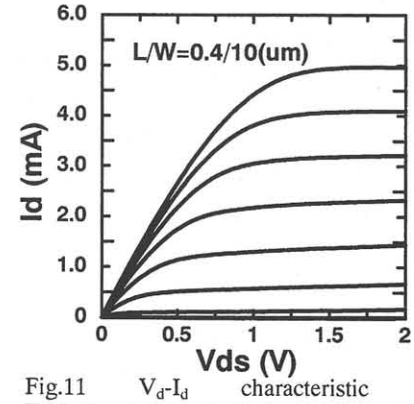

Fig.11 V_d-I_d characteristic of $TaN_X/Ta/TaN_X/TaO_X/Si_3N_4/Si$ structure FD-SOI MISFET.