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Studies of AlGaN/GaN High Electron Mobility Transistors on Semi-Insulating Silicon Carbide and Sapphire Substrates

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1. Introduction

Significant progress has been made in the development of AlGaN/GaN based field effect transistors on bulk GaN,[1] sapphire,[1-5] n-type & p-type and semi-insulating (SI) SiC[1,6-8] substrates for high-speed, high-power and high-temperature applications. For high-power operation, the thermal conductivity of the substrate is expected to be an important design issue and the relatively poor thermal conductivity of sapphire is expected to limit the device output power. Silicon carbide on the other hand, has an excellent thermal conductivity and is an obvious choice for a substrate when thermal considerations are important. The characteristics of HFET fabricated in bulk GaN substrate is not much superior than SiC and sapphire based HFET structures.[1] Some authors have fabricated the HEMT's on SI-SiC substrates and also simply compared with the HEMT's on sapphire substrate.[1,6,8] In this article, we report the fabrication and dc characteristics of AlGaN/GaN HEMT's on SI- SiC and sapphire substrate with maximum dc transconductance (g_{mmax}) values of 291 and 166 mS/mm, respectively. We also present the comparative studies between the HEMT's on SI-SiC and sapphire substrates.

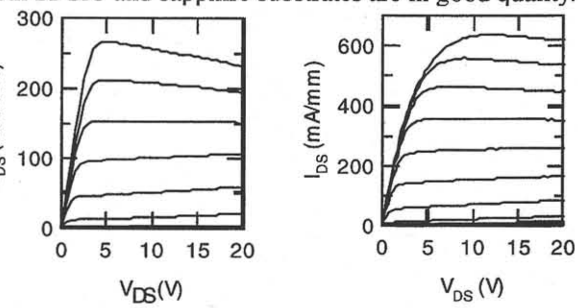
2. Experimental

The AlGaN/GaN layers were grown on (0001)-oriented SI-4H-SiC and sapphire substrates using atmospheric pressure MOCVD (Nippon Sanso, SR-2000). The device structure consists of 3 nm undoped AlGaN barrier layer, 15 nm silicon doped AlGaN supply layer, 7 nm undoped AlGaN spacer layer, 3000 nm insulating GaN layer (i-GaN) and a 200 nm AlN buffer layer on top of the SiC substrate. For the sapphire substrate, instead of AlN buffer layer, undoped GaN layers were used as a buffer layer. The Al contents of AlGaN layers were maintained at 26%. Hall effect measurements were carried out on these structures at 300 and 77 K using van der Pauw configuration. To understand the surface morphology of the grown layers, Atomic Force Microscopy (AFM) was used with the scan area of 1 μm^2.

The device isolation was accomplished by mesa dry etching down to i-GaN by BCl_3 plasma reactive ion etching.[2] The ohmic contacts were performed by the deposition of a Ti/Al/Ti/Au (25/100/45/55 nm), which was subsequently alloyed at 750°C for 60 s in N_2 atmosphere. The gate-metal Pd/Ti/Au (40/40/80 nm) was optically defined 2, 2.2, 3.0 and 5 µm long gates using optical lithography through conventional lift-off method. Both ohmic and gate metals were evaporated using Electron Beam evaporation system. The dc characteristics were measured using HP4145B semiconductor parameter analyser. To measure the 2 DEG channel depth (d_{2DEG}), capacitance-voltage (C-V) measurements were carried out on Schottky diodes at 1 MHz using HP4845 LCR meter.

3. Results and discussion

The HEMT's dc, Hall, C-V and surface parameters of AlGaN/GaN heterostructures grown on SI-SiC and sapphire substrates are shown in Table 1. The AlGaN/GaN heterostructure grown on SI-SiC substrates show high value of carrier mobility and sheet carrier density compared with AlGaN/GaN heterostructure grown on sapphire substrate. This can be explained through lattice mismatch between GaN and the respective substrates. The high values of sheet carrier density ($\geq 10^{13}$ cm^{-2}) indicate that the MOCVD grown AlGaN/GaN heterostructures on both SI-SiC and sapphire substrates are in good quality.



(a) (b)

Figure 1. I_{DS}-V_{DS} characteristics of 200 µm wide gate HEMT's on (a) sapphire and (b) SI-SiC substrates. V_{GS}=-2.5 to 1.5 V with 0.5 V steps

Table 1. The device dc, Hall, C-V and surface parameters of AlGaN/GaN HEMT's. The values within the bracket are measured at 77 K

Parameters	HEMT's on SI-SiC		HEMT's on sapphire	
	15 µm	**200 µm**	**15 µm**	**200 µm**
g_{mmax}(mS/mm)	291	216	166	125
I_{DMAX}(mA/mm)	847	635	440	260
R_s (Ω-mm)	1.59	2.16	2.79	3.65
V_{th} (V)	-2.4	-2.7	-2.0	-2.1
L_g (µm)	2.2	2.2	2	2
L_{sg} (µm)	1.8	0.3	2.0	0.5
L_{sd} (µm)	8.5	5	8.5	5
n_{C-V} (cm^{-3})	3.99×10^{19}		1.85×10^{19}	
d_{2DEG} (nm)	17.75		22.66	
n_s (cm^{-2})	1.2×10^{13} (1.1×10^{13})		$1.0x^{13}$ (1.0×10^{13})	
μ_H (cm^2/Vs)	1281 (5351)		1163 (5121)	
R_C (Ω-mm)	2.33		3.92	
Rms (nm)	0.38		0.86	
P-V (nm)	2.85		7.33	

Figure 1 a) and b) shows the I_{DS}-V_{DS} characteristics of 200µm wide gate AlGaN/GaN HEMT's on SI-SiC and sapphire substrates, respectively. The drain-source current reduction has been observed in both the substrate grown 200 µm wide gate HEMT's. But the SiC substrates grown HEMT's are showing less drain current reduction (3%)

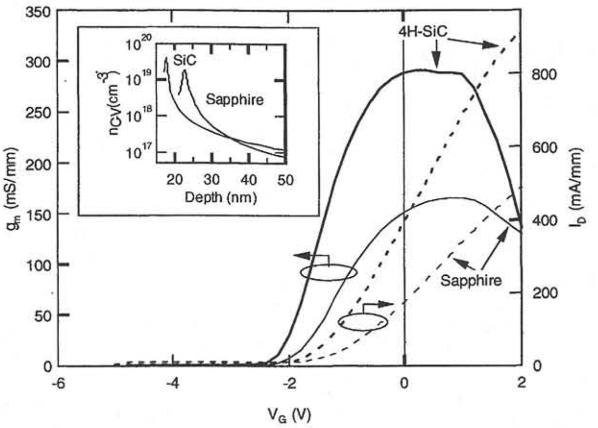


Figure 2. Transfer characteristics of 15 μm wide gate HEMT's on sapphire (L_g=2 μm) and SI-SiC (L_g=2.2 μm) substrates. Inset Figure: C-V profile of HEMT's on SiC and sapphire substrates. V_{ds}=-6V

compared with the HEMT's on sapphire substrates (13%). Thermal conductivity of the sapphire substrate (0.5 $Wcm^{-1}K$) is one order lower than the SiC substrate (1.3 $Wcm^{-1}K$). Self-heating is not affected very much for SiC based HEMT's. Little high value of contact resistance has been observed for the HEMT's on sapphire substrate (3.9Ω-mm) compared with the HEMT's on SI-SiC substrate (2.3Ω-mm). The observed contact resistance values are one order higher than the reported values.[3,5,7] The breakdown voltages of SiC based and sapphire HEMT's are greater than 100 and 50 V, respectively.

Figure 2 shows the transfer characteristics of 15 μm wide-gate HEMT's on SI-SiC and sapphire substrates. The values of g_{mmax} and maximum drain-source current density (I_{Dmax}) are shown in Table 1. The g_{mmax} of 291, 166 mS/mm with maximum drain-source current density of 847, 440 mA/mm has been observed for the HEMT's on SI-SiC and sapphire substrates, respectively. To our knowledge, this is the highest g_m value ever reported for 2.2 μm long and 15 μm wide gate HEMT's on SI-SiC substrates. The values of g_{mmax} and I_{Dmax} are ≈50% more for HEMT's on SiC substrates with respect to HEMT's on sapphire substrates (see table 1). From this we understand that the AlGaN/GaN heterostructures grown on SI-SiC substrates are in good quality compared with the heterostructures grown in sapphire substrates. This has been confirmed with the AFM and C-V profiling measurements.

Figure 3 shows the g_{mmax} versus gate-lengths for HEMT's on SI-SiC and sapphire substrates. The extrapolated g_{mmax} values (towards low gate lengths) are high compared with the reported values.[3-4,6-8] This is due to the good quality AlGaN/GaN heterostructure on SI-SiC substrate. Large ionized carrier density (n_{C-V}) with low d_{2DEG} has been observed for HEMT's on SI-SiC compared with HEMT's on sapphire substrates (see Table 1). Moreover, the C-V profile peak FWHM of HEMT's on SI-SiC (≈0.55nm)is low compared with the HEMT's on sapphire (≈1.18nm) substrates. From this we understand that the SiC based HEMT's gave large charge confinement with narrow channel. Low values of Rms surface roughness and peak-valley (*P-V*) has been observed for HEMT's on SI-SiC substrates. This is due to the small lattice mismatch between SiC and GaN, so one might expect the dislocation density of HEMT's on SiC to be lower. From these results, it is clear that the material properties and device characteristics of HEMT's on SiC substrates are superior to HEMT's on sapphire substrates.

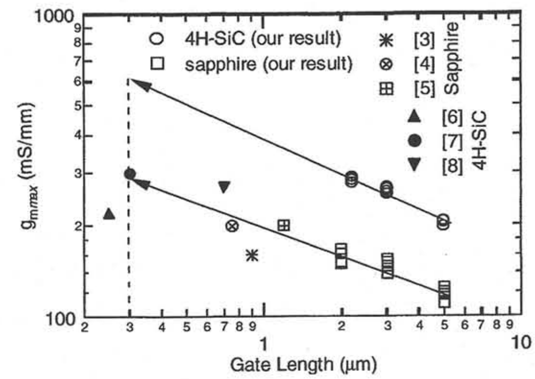


Figure 3. Maximum dc extrinsic transconductance (g_{mmax}) as a function of gate lengths for HEMT's on sapphire and SiC substrates.

4. Conclusion

The fabrication and performance of MOCVD grown $Al_{0.26}Ga_{0.74}N$/GaN high electron mobility transistors on sapphire and SI-SiC substrates are reported. High values of both Hall sheet carrier and ionized carrier densities demonstrate the grown AlGaN/GaN heterostructures are in good quality. The g_{mmax} of 291, 166 mS/mm with I_{Dmax} of 847, 440 mA/mm has been observed for the HEMT's on SI-SiC and sapphire substrates, respectively. To our knowledge, this is the highest g_m value ever reported for 2.2 μm long and 15 μm wide gate HEMT's on SI-SiC substrates. The values of g_{mmax} and I_{Dmax} are ~50% more for HEMT's on SiC substrates with respect to HEMT's on sapphire substrates. Though the 200 μm HEMT's on SiC substrates are showing drain-source current reduction (3%) for gate voltage of +1.5 V, the drain current reduction is much less than the HEMT's on sapphire substrates (13%). The current carrying capability with high g_m and thermal management of HEMT's on semi-insulating SiC substrate are superior to HEMT's on Sapphire substrates.

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