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A New Two-Step Round Oxidation STI Technology for Highly Reliable Flash Memory

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1. Introduction

Scaling of the Shallow Trench Isolation (STI) pitch keeping integrity of tunnel oxide is indispensable for realizing high density flash memory[1]. Stress reduction in STI is one of the key issues of scaling STI pitch [2]. Some approaches such as mini-LOCOS method [3] or high temperature oxidation after filling field oxide [4] have been carried out to manage Si corner issues. However, for the flash memory applications, corner smoothing and the stress induced by growing oxide are still marginal in these methods. This paper describes the new 2-step round oxidation technology for highly reliable flash memory process. This is a simple and quite effective solution to realize extremely smooth corner profile with reduced stress, and exhibits excellent charge-to-breakdown (Qbd) comparable to the LOCOS process with high scalability, despite the gate overlapping on the trench edge. Finally, we show superior flash memory reliability, such as erased Vth distribution, charge retention, and endurance characteristics of NOR flash memory by this technology. This 2-step oxidation STI technology is capable of 256Mbit NOR flash memory.

2. STI Process Sequence

Fig.1 shows the proposed STI process sequence for the flash memory. Sacrificial (1^{st}) trench oxidation and HF dip, which are keys to control integrity of the STI edge, followed by 2^{nd} round oxidation in 1100℃ Dry O_2 ambient is performed inside the trench of 275nm depth. Then, the trench is filled with High Density Plasma (HDP) CVD oxide and planarized by CMP. Capacitors and NOR type flash memory arrays were fabricated.

3. Results and Discussions

TEM photograph of the conventional STI edge partially shows rugged profile in Fig.2(a). While, the proposed STI provides very smooth profile with enough corner radius of ~40nm (Fig.2(b)). More advantage of this method is effective corner rounding with the same oxidation amount as shown in Fig.3. Stress simulation at the round oxidation is shown in Fig.4. High compressive stress concentrates at the Si corner by the conventional STI. However, the proposed process, which prepares enough room for growing round oxide at the corner, results in minimized stress. This difference strongly affects to the above TEM profiles. Moreover, remarkable improvement in Qbd characteristics with the proposed process are observed especially on STI edge intensive structures (Fig. 5). The poor Qbd of the conventional STI is caused by the enhanced tunneling current at the sharp corner partially formed on the edge. The STI edge Qbd degrades as active dimension scaling less than 0.3μm with sacrificial trench oxide of 25nm (Fig.6 (a)). By the optimized sacrificial trench oxide of 14nm, the scalability of Qbd is so improved that no degradation of Qbd up to the active width of 0.20μm, which is applicable to 0.13μm generation NOR flash memory (Fig.6 (b)). The sacrificial trench oxidation can improve the integrity of scaled active area by stress reduction in the trench oxidation, not only by its smooth corner profiles. Despite the gate overlapping on the trench edge, the proposed corner effect suppression in Qbd is as excellent as the LOCOS process. Erased Vth distribution, representing tunnel current uniformity of the flash cells, with the proposed STI is controlled within 1.5V range tightly as the LOCOS process (Fig.7). Even after 100k P/E cycling stress, program and erase time degradation by trapping is controlled as negligibly as the LOCOS (Fig. 8). The charge loss prevention of 64Mbits cell array in 250℃ bake is satisfactory with the proposed STI (Fig. 9).

4. Conclusion

Newly proposed 2-step round oxidation method have been developed for highly reliable and high density flash memory and successfully implemented into 64M NOR flash memory. This technology has shown high immunity of corner rounding stress and very smooth corner shape, which result in satisfying integrity of flash memory, such as excellent Qbd and superior flash array performance and reliability equal to the complete LOCOS process.

References

[1] H. Watanabe et al,. IEDM, p833 (1996)
[2] T. Kuroi et al., IEDM, p141 (1998)
[3] A. Chatterjee et al,. IEDM, p829 (1996)
[4] C. P. Chang et al,. IEDM, p661 (1997)

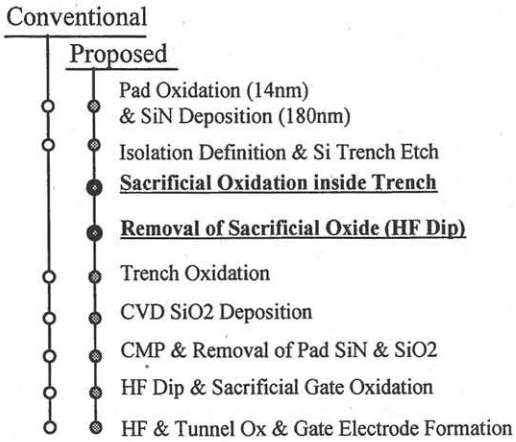

Fig.1 Process steps of the proposed 2–step oxidation STI, and the conventional method.

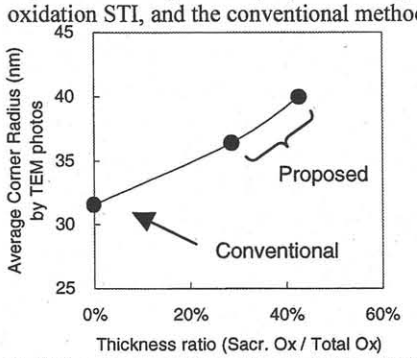

Fig.3 STI corner rounding effect on the sacrificial oxide ratio with a total oxide amount of 50nm.

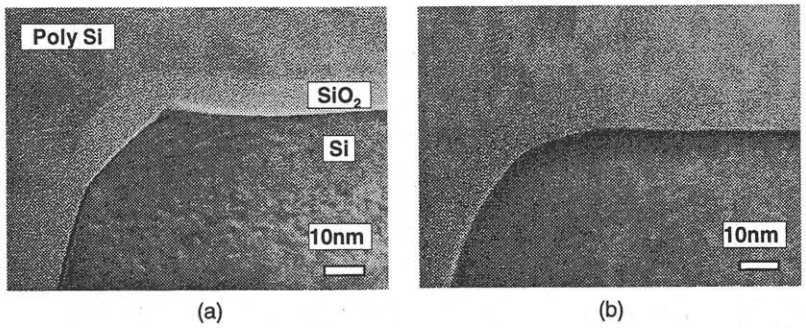

Fig.2 Cross sectional TEMs of the top corner on active Si edge after gate electrode formation. (a) conventional STI and (b) the proposed STI with 2–step oxidation.

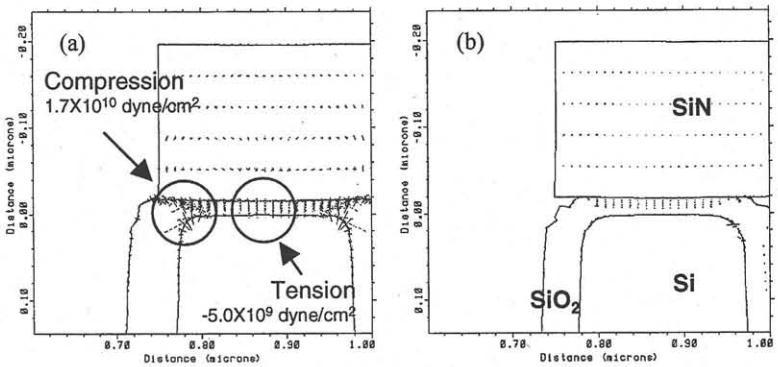

Fig.4 Stress simulation results after round oxidation, performed with TSUPREM - 4. (a) Conventional round oxidation 50nm, (b) 2-Step oxidation with amount oxidation of 50nm.

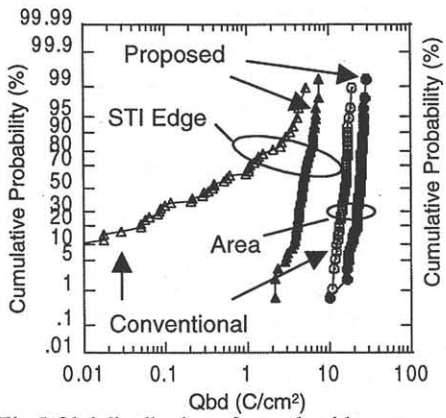

Fig.5 Qbd distribution of tunnel oxide grown on conventional and the proposed STI. Tunnel oxide thickness is 10.5nm, Jstress= 1A/cm²

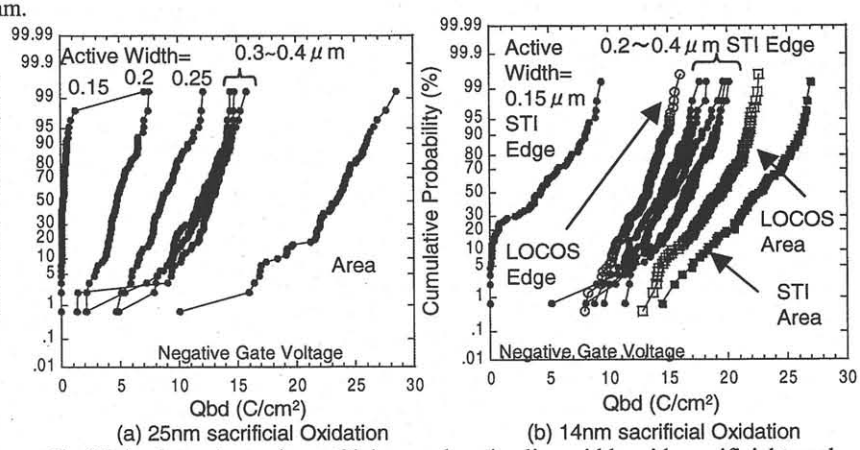

Fig.6 Edge intensive and area Qbd on each active line width, with sacrificial trench oxidation thickness of (a) 25nm, (b) 14nm. Tunnel oxide thickness=10.5nm, Jstress= 1A/cm², STI Edge length= 355mm. (b) compares the optimized STI and the LOCOS.

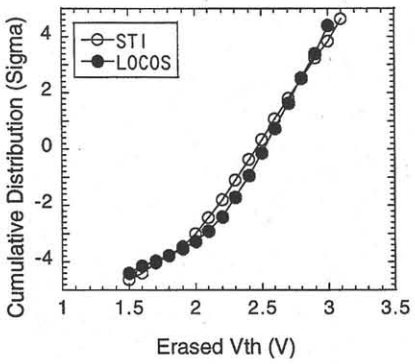

Fig.7 Block Erased Vth distribution of NOR flash memory array by LOCOS Process and the proposed STI Process. Block size : 512k bits.

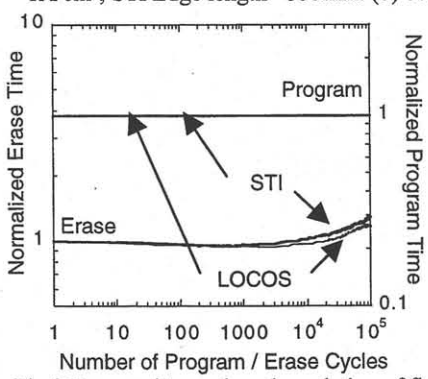

Fig.8 Program/Erase time degradation of flash cell array (512k bits a block) after cycled stress by LOCOS Process and the proposed STI Process. CHE Program and F-N Erase.

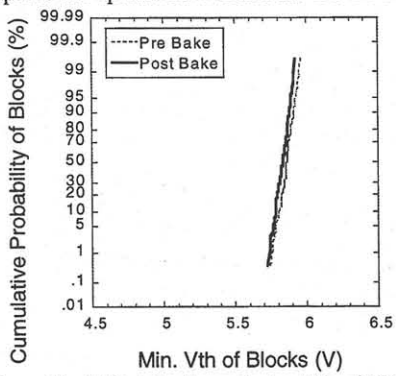

Fig.9 Distribution of min. Vth of 125 blocks (512k bits/a block) of flash array, before and after 250℃ 72h Bake, with the proposed STI Process.