Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 542–543

C-10-3

Macro Gate Current Model and Modeling Parameter Extraction of the SSI Flash Cell

Chun-Mai Liu, Ming-Bing Chang, Ping Guo, Albert V. Kordesch, Ben Lee and Kung-Yen Su

Winbond Electronics Corporation of America, 2727 North First St., San Jose, CA 95134, USA (408-544-1773; fax 408-544-1786; cmliu0@winbond.com.tw)

Introduction

The source-side-injection (SSI) flash memory cell has been recently employed as the base of a multilevel storage technology [1, 2]. In order to optimize the programming circuit for a multilevel flash memory, an accurate circuit model of the cell is required.

The SSI flash cell consists of a select gate transistor and a floating gate transistor merged in a split-gate configuration as is in Fig. 1. In a two-transistor framework, the gate voltage of FG (floating gate) transistor is found well represented by linear capacitive couplings of Vsg (select gate, the same as WL), Vcs (common source), Vc (common node) and Vb (substrate) under READ condition [3]. TCAD simulations and experimental data prove this framework is extendable into PROGRAM condition [3]. Moreover a rigorous procedure of transistor parameter extraction for FG and SG has been developed [4]. The concept of fixed coupling capacitance ratios leads us to our basic cell macro as is in Fig. 2, which uses voltage controlled voltage sources and charging capacitor to generate Vfg. The current source Ifg is used to account for the floating gate charging effect by the SSI electrons. In this work, we have devised a macro gate current model based on the original Lucky-electron model developed for transistor gate current [5] to extend the two-transistor macro cell model into program condition. Then using a rigorous procedure, the gate current model parameters were extracted. The behavior of macro model has been verified with measurements over the range of operation of a normal cell.

Models of Gate Current

Split-gate flash cells make use of the high electric field at the split point between the two gates to inject electrons into the floating gate [6-8]. According to the Lucky Electron Model [5, 8], the gate current, Ig, can be written as follows:

$$I_g = C_0 I_d \left(\frac{\lambda E_m}{\Phi_b} \right)^2 \exp \left(\frac{-\Phi_b}{\lambda E_m} \right) \qquad (1)$$

Here C_0 is a constant, I_d the drain current, λ the electron mean free path, E_m the peak electric field, and Φ_b the effective barrier height[1] for electron injection into the gate oxide.

For this three terminal SSI cell, under program condition the FG and SG transistors are both in saturation[2], and a high field is set between the transistors as shown in Fig. 3, where the channel current spreads away from the surface when crossing the gap between the transistors. This entails that the gate drive of the FG transistor is near constant when I_{bit} (= Id, bit line current) is fixed. The two-transistor cell model shows the virtual source voltage[3] of FG, Vc, is tracking Vfg, namely, Vc ~ Vfg. E_m is proportional to (Vc – Vdsat_sg)/t_gap, where t_gap is a characteristic length of the gap region between SG and FG transistors.

Consequently, a macroscopic model gate current can be written as:

$$I_g = C_1 I_{bit} \left(\frac{V_{fg} + k_1 V_{cs} + B_{sg}}{C_2} \right)^2 \exp \left(\frac{-C_2}{V_{fg} + k_1 V_{cs} + B_{sg}} \right) \qquad (2)$$

Here C_1 and C_2 are constants, the k_1Vcs term corresponds to the CS DIBL effect. Bsg is a constant including Vsg, Vtsg and Vtfg. The effects of E_{ox} and of E_m are approximated[4] by $-C_2/(V_{fg} + k_1 V_{cs} + B_{sg})$.

Experimental and Results

We derived the gate current from the programming behavior of a real cell. Vsf (source-follower voltage) vs. tp (program time) data are collected then transformed by a procedure as illustrated in Fig. 4, to the gate current Ig vs. floating gate voltage Vfg_program curve as shown in Fig. 5. This data has exhibited the typical Lucky-electron like characteristics, where the Vcs dependence is observed. Then by means of Eq. (2), the parameter k_1, the constants C_1 and C_2 are determined. Fig. 6 shows the gate current model Ig play back (I_{bit} = 1uA, Vsg = 2.3V and substrate bias V_b = 0).

Next we investigate the dependence of Igr (=Ig/I_{bit}, relative gate current) on I_{bit} and the effect of substrate bias using a constant current programming technique [9]. The shift in floating gate voltage can be determined precisely from ΔVsf. The gate current, Ig, should be directly proportional to the bit-line current, I_{bit}. However, the increased current may increase the vertical field Ey and oxide field Eox, then the lowered oxide barrier increases the electron injection efficiency.

Fig. 7 shows the shifts of Vsf (~Qfg, FG stored charge) of the cumulative programming curves with several programming currents (Ip = I_{bit}) where the program interval Δtp are adjusted such that Ip*Δtp remain unchanged. In this way, the effect of I_{bit} on Igr can be directly observed. Here the measured Vsf decreases linearly as ln(I_{bit}) increases with the same rate at two Vcs voltages. To the first order, this effect can be included as a shift of the Igr vs. Vfg curve along the ln(Igr) axis.

Similarly the gate current is enhanced by back bias as in Fig. 8. Here the measured Vsf decreases linearly as Vsub decreases (more negative) with nearly the same rate at several Vcs voltages. Again this effect can be included as a shift of the Igr vs. Vfg curve along the ln(Igr) axis. The gate current can be modified empirically as[5]:

$$I_g = C_1 I_{bit} \left(\frac{V_{fg} + k_1 V_{cs} + B_{sg}}{C_2 - \Delta_1 \ln I_{bit} + \Delta_2 V_b} \right)^2 \exp \left(\frac{-C_2 + \Delta_1 \ln I_{bit} - \Delta_2 V_b}{V_{fg} + k_1 V_{cs} + B_{sg}} \right) \qquad (3)$$

Here Δ_1 and Δ_2 are constants empirically determined, I_{bit} in uA, V_b the substrate bias.

The substrate bias effect also shows up when Vsg is changed. The effect of Vsg can be modeled by change of voltage reference in Eq. (3).

Fig. 9 shows the simulation vs. measurement for a variety of programming conditions. Fig. 10 shows the simulation vs. measurement for accumulative programming data [1].

The temperature effect was also studied. The high temperature Vsf read were first translated to room temperature Vsf read [1], then the gate current is extracted as shown in Fig. 11. Figure 12 shows Ig vs. 1/T. The effect can be characterized as Ig = Ig_0*exp (C_3/T). We observed that gate current doubled in every ~48C. This is higher than that reported for the drain side hot electron injection [5].

Conclusions

In this work, we have presented a new circuit simulation macro model, including an empirical formula for gate current, which accurately represents the behavior of a split-gate SSI flash cell during the programming event. This model has been used successfully to design commercially available analog multilevel flash storage devices.

Acknowledgments

We would like to thank Winbond management for their support and encouragement. We also thank Kai-Man Chan for TCAD support.

1 $\Phi_b = \Phi_{b0} - 2.59 * 10^{-4} Eox^{1/2} - a_0 Eox^{2/3}$ [8].

2 While for HIMOS, the FG transistor operates in linear region [8].

3 Here Vc is not a well-defined point, the FG and SG cannot be clearly demarcated.

4 We note that the effects of both Em and Eox are lumped into the denominator.

5 Since TCAD simulations show significant Ey variations (so is Eox) as a Ibit and Vb are varied, while the Ex changed little, the correction terms are entered into the numerator of the exponent.

References

[1] C.-M. Liu, et al., *Proc. of VLSI-TSA*, pp. 187, 1999.
[2] C.-M. Liu, et al., *Extended Abstract of SSDM*, September, pp. 542, 1999.
[3] C.-M. Liu, et al., *Extended Abstract of SSDM*, August, pp 288, 2000.
[4] S.-P. Sim, et al., *SISPAD2001*, September, 2001, to be presented.
[5] Simon Tam, et al. *IEEE Trans. Electron Devices*, vol. ED-31, no. 9, pp. 1116, 1984.
[6] Albert T. Wu, *Ph. D. Dissertation*. EECS, UC Berkeley, May 1987.
[7] Jan F. Van Houdt, et al., *IEEE Trans. Elect. Dev.*, vol. ED-40, no. 12, pp. 2255, 1993.
[8] Jan F. Van Houdt, et al., *IEEE Trans. Elect. Dev.*, vol. ED-42, no. 7, pp. 1314, 1995.
[9] C.-M. Liu, et al., *Proc. of NVSMW*, pp. 81, 2000.

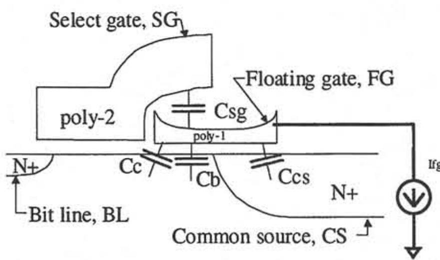

Fig. 1 The SSI flash cell--two transistors in a split-gate configuration with four components of FG capacitance and a current source for Ifg.

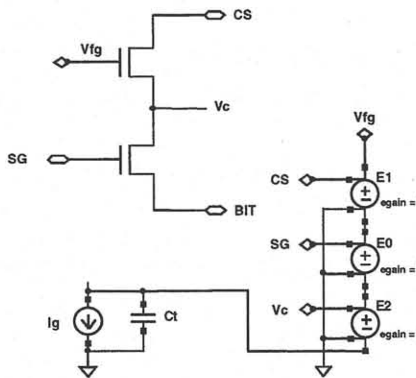

Fig. 2 Cell macro based on the two-transistor framework— voltage controlled voltage sources and a current source for Ifg.

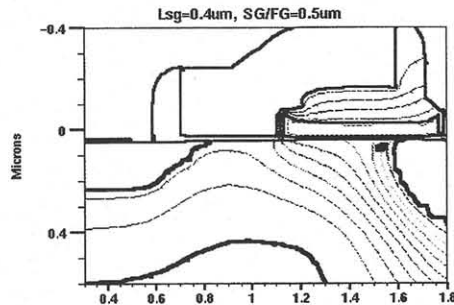

Fig. 3 The equipotential lines in the SSI flash cell showing the high field region at the split point.

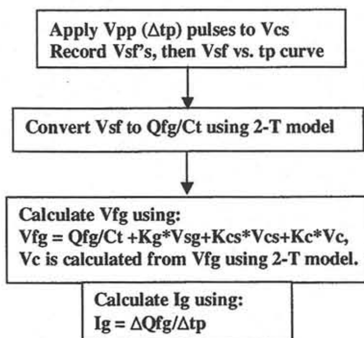

Fig. 4 Flow diagram Illustrates the procedure to extract gate current and the corresponding Vfg.

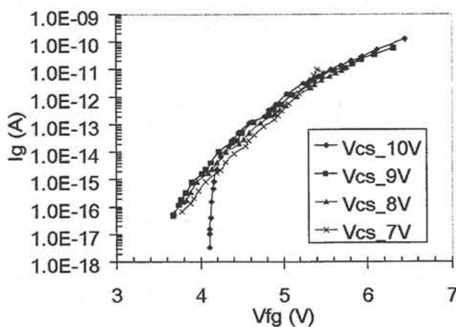

Fig. 5 Flash Cell Gate Currents Extracted From Programming Curves (Ibit = 1uA).

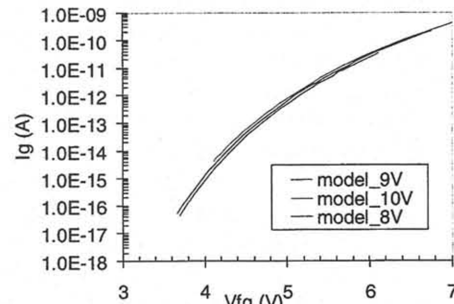

Fig. 6 Gate Current Model play back (I_{bit} = 1uA)

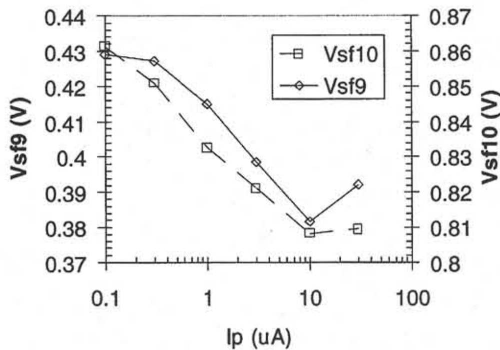

Fig. 7 Vsf at Vcs=9V, and Vcs=10V from Accumulative Programming Curves vs. Programming Current Ibit.

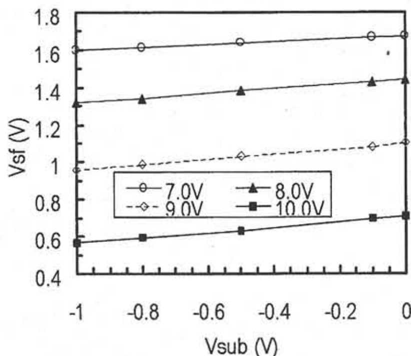

Fig. 8 Vsub Effect on Programming. (the 7.0V, 8.0V, 9.0V and 10.0V refers to Vcs voltages in the respective cumulative programming curves.)

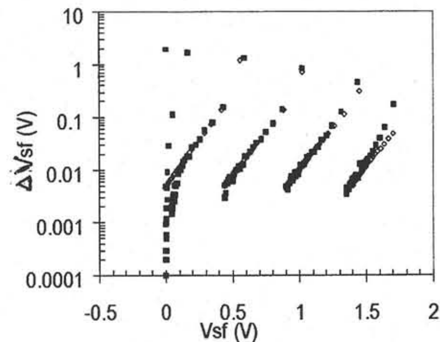

Fig. 9 Spectre Simulation Results with Gate Current: Model (open dots) vs. Measured Programming Curves (solid dots), Vcs=7 to 12 V, Vcs step=1V; Dt=10us; Ibit=10uA

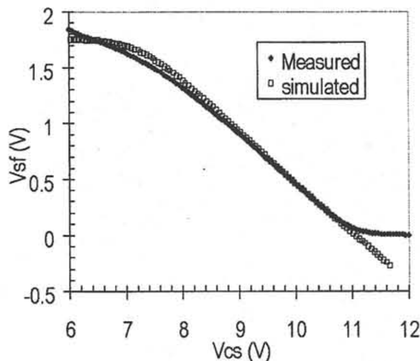

Fig. 10 Accumulative Programming Curves: Measured vs. Simulated.

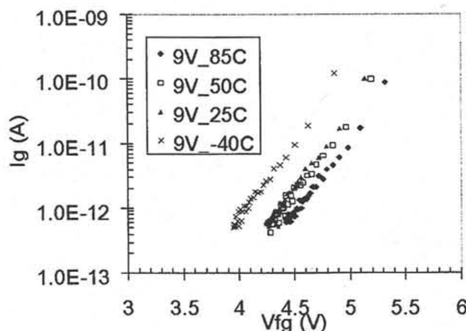

Fig. 11 Flash Cell Gate Current over Temperatures with Vcs=9V.

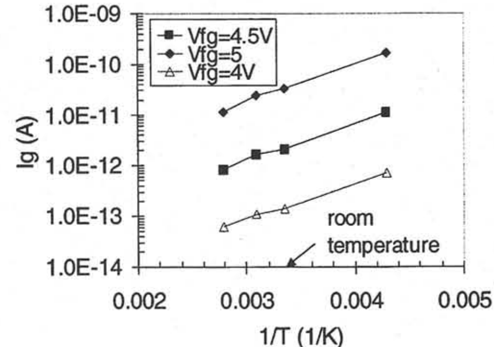

Fig. 12 Gate Current vs. 1/T at various Vfg.