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A New Two-Transistor MACRO Modeling of Source Side Injection (SSI) Flash Cell Considering Remote-Electrode Induced Barrier Lowering (RIBL)

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1. Introduction

Source Side Injection (SSI) Flash cell has drawn much attention during the past few years for its high injection efficiency and low programming current [1, 2]. To optimize the cell operation and to facilitate the array control circuit design, better understanding of the cell behavior and accurate prediction of the I-V characteristics are essential. Though series-connected 2 transistors with an appropriately coupled floating gate is natural description for the SSI cell, there has been no general procedure of parameter extraction since the 2 transistors configuration makes it extremely difficult to extract physical and accurate parameters of the transistors independently. Also there should be a consideration on the interaction between the two transistors especially for deep sub-micron cell because they are located physically closely. In this paper, we present a methodology to create a MACRO model for a split-gate Flash cell, including the interaction between the two transistors.

2. MACRO Cell Representation of SSI Cell

Fig. 1 shows a cross-sectional TEM view of our three-poly split-gate Flash cell with its operating parameters. The cell is approximated by a representation of series-connected 2 transistors with a floating gate as shown in Fig. 2. Here the floating gate is coupled to other electrodes as follows.

$$\Delta V_{FG} = \sum \alpha_i \Delta V_i + \Delta Q_{FG} / C_{total} \qquad (1)$$

where coupling ratio is defined as $\alpha_i = C_i / C_{total}$ for each coupling node; CS, V, CG, SG and B. Device simulation shows that the 2 transistors representation is reliable under most operating conditions except when both transistors are in deep saturation. Here current flows penetrate deep into the bulk between SG and FG, and the node "*V*" is not well defined physically and hence is a virtual node. The dotted line in Fig. 2 is used to indicate the effect of remote electrodes on M_{SG}, which will be discussed later.

3. Parameter & Coupling Ratio Extraction

The series-connected transistor configuration makes it difficult to extract parameters of one transistor independently of the other. Moreover, for each component transistor, one of the junctions is arbitrary defined and results significantly different DIBL & body effect from its stand-alone counterparts [3]. To overcome the difficulty in parameter extraction, divide and conquer strategy shown in Fig. 3 is used. First we extracted a full set of BSIM3 parameters for M_{SG} and M_{FG} via their respective groups of stand-alone transistors. Then using the accessible gate cell[1)], key parameters of each component transistor M_{SG} and M_{FG}: effective channel length, body effect, DIBL, and channel length modulation are extracted[2)]. Then the 2 sets of parameters are combined to yield an optimized parameter set to fit the split-gate transistors I-V characteristics using a commercial parameter optimizer UTMOST. The coupling ratios (CR's) were extracted by a method based on source follower voltage (V_{sf}) measurement [4] as illustrated in Fig. 4. After a final tuning of BSIM3 parameters and CR's with measured I-V data for the floating gate cell, a full parameter set is attained. Using the parameter set, our MACRO cell implemented in SPICE was confirmed by comparison with measurement as shown in Fig. 5 and Fig. 6.

4. Remote-electrode Induced Barrier Lowering (RIBL)

Although the I-V and V_{sf} data yield good agreement between measurement and simulation, we find that the effect of remote electrodes on M_{SG} should be considered because small change in the V_{th} of M_{SG} can induce significant error in programming current, I_{CS}. The deficiency of 2-transistor model for the split-gate cell can be supplemented by including this Remote-electrode Induced Barrier Lowering (RIBL), which will be more important as the Flash cell scales downwards. Using an accessible gate cell, respective contribution of CS and FG on this V_{th} lowering is measured as V_{sf} (~ $-V_{th}$) in Fig. 7. Deep junction, though, CS is for high voltage endurance, FG shows stronger effect than CS because it is electro-statically closer to M_{SG}. To include the RIBL effect, the following empirical equation is used.

$$V_{SG,int} = V_{SG} + \beta_{FG} V_{FG} + \beta_{CS} V_{CS} \qquad (2)$$

$$\beta_i = \gamma_{i1} + \gamma_{i2} V_{SG} \qquad (3)$$

where the gate voltage of M_{SG} ($V_{SG,int}$) is given as a superposition of external SG voltage (V_{SG}) and RIBL effect by FG and CS. The coefficient of RIBL, β_i, has a strong dependency on V_{SG} (see Fig. 8) and approximated as in Eq. (3) with constant γ_{ij}. With the inclusion of the RIBL effect, V_{th} of M_{SG} is more accurately fitted as shown in Fig. 9[3)].

5. Conclusions

We presented a SPICE-compatible MACRO model of a SSI Flash cell based on a methodology of practical cell partitioning and a systematic and rigorous parameter extraction scheme. Including RIBL effect for the first time, we arrived at a more physical and reliable 2-transistor model.

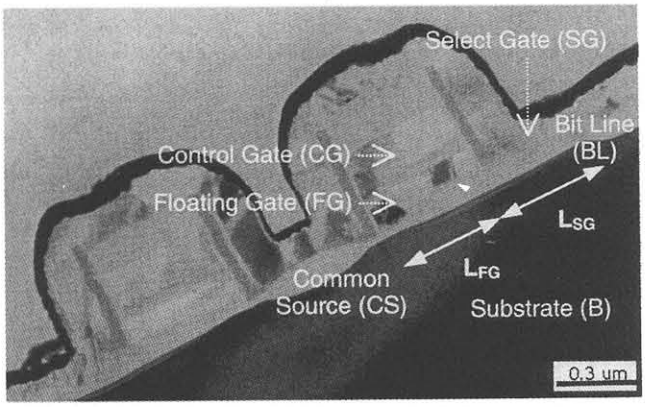
References

[1] S. Kianian, et al., VLSI Tech Symp., 1994, p.71
[2] Chun-Mai Liu, et al., VLSI Tech. Symp., 1999, p.187
[3] Sang-Pil Sim, et al., SISPAD, 2001, to be presented.
[4] Chun-Mai Liu, et al., Ext. Abs. of SSDM, 2000, p.288

[1)] In accessible gate cell, FG and CG are tied.

[2)] By device simulation, in which we can exclude arbitrarily the effect of the series transistors, these parameters of the CT are shown to be mostly different from those of stand-alone transistors.

[3)] For the floating gate cell, V_{CS} sweep entails RIBL by FG through the coupling between FG and CS as well as by CS.



	V_{SG}	V_{CG}	V_{BL}	V_{CS}	V_B
Write	1.0[V]	10[V]	0.0[V]	5.0[V]	0.0[V]
Erase	0.0[V]	-10[V]	Open	5.0[V]	0.0[V]
Read	3.3[V]	1.2[V]	1.2[V]	0.0[V]	0.0[V]

Fig. 1: Cross-sectional TEM photography of SSI Flash cell and operating conditions. L_{SG} = 0.5μm, L_{FG} = 0.4 μm.

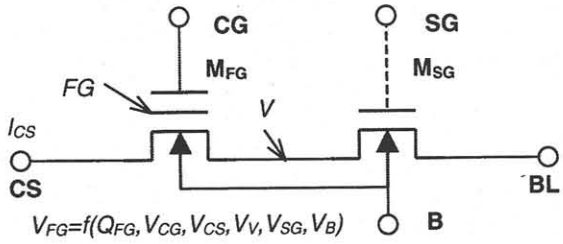


Fig. 2: Equivalent MACRO cell of SSI Flash cell. *V* represents a virtual node between the two transistors. V_{FG} is coupled by 5 capacitors between CG, CS, V, SG, B. Dotted line on M_{SG} is intended to represent the effect of remote electrodes on M_{SG}.

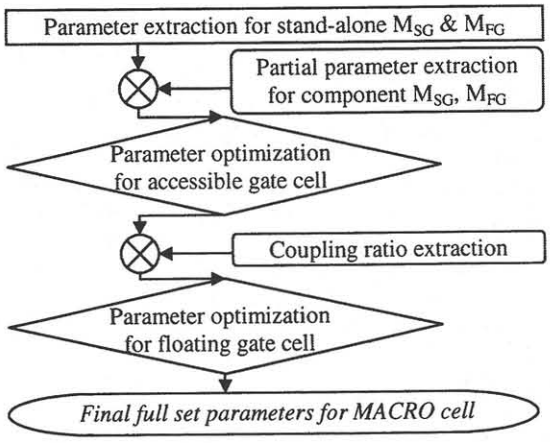
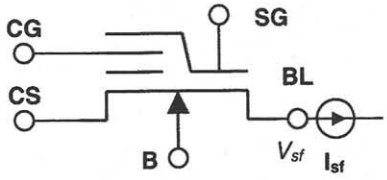


Fig. 3: Flow chart diagram for parameter extraction.



α_{SG}	0.12
α_{CG}	0.56
α_V	0.14
α_{CS}	0.15
α_B	0.03

Fig. 4: Illustration of CR extraction technique and extracted CR's. Here V_{sf}, the voltage read at constant current source I_{sf}, is used to get V_{FG} by the relationship, $V_{sf}=V_{FG}-V_{th}$ of M_{FG}. The CR's are extracted at " READ" condition and assumed to be constant.

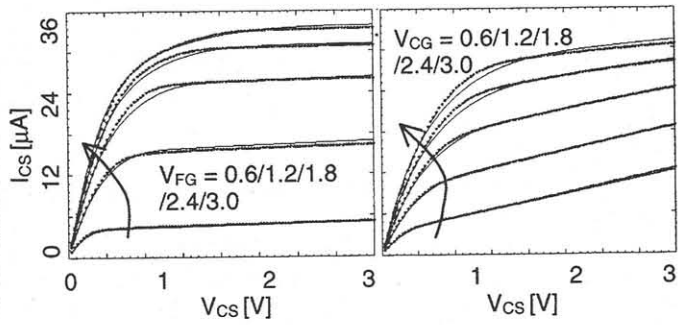


Fig. 5: I-V characteristics: measurement (solid line) and SPICE simulation (dotted line) for accessible gate cell (left) and for floating gate cell (right) at $V_{BL} = V_B = 0$, $V_{SG} = 1.2V$.

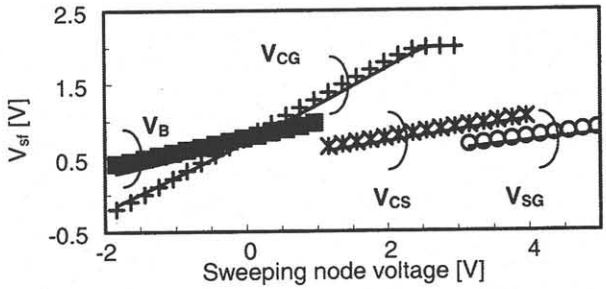


Fig. 6: Coupling of V_{FG}, represented here by V_{sf}, from other electrodes: measurement (symbols) and SPICE simulation (line).

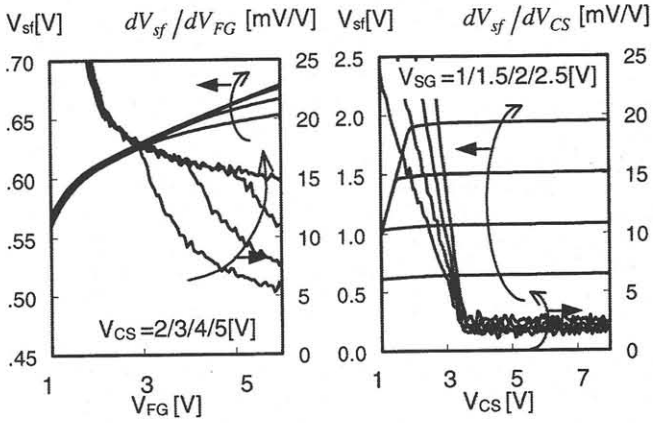


Fig. 7: V_{th} of M_{SG} monitored by V_{sf} for an accessible gate cell: V_{FG} sweep with V_{SG}=1V (left) and V_{CS} sweep with V_{FG}=4V (right).

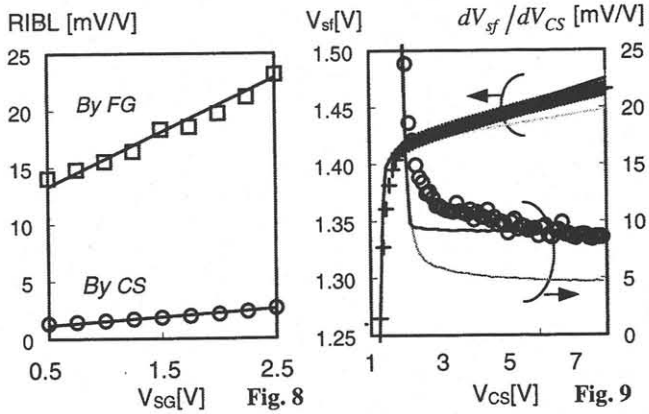


Fig. 8: V_{SG} dependence of RIBL at programming condition (V_{CS}=5V): measurement-symbol, approximation-line.

Fig. 9: V_{th} lowering by VCS for a floating gate cell: measurement-symbol, simulation with RIBL-black line & without RIBL-gray line.