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A Novel Method for Extracting the Coupling Coefficient without a Reference Cell for a Split-Gate Flash EEPROM

H. Fujiwara, M. Arimoto, T. Kaida, S. Sudo, K. Kurooka, M. Hirase, T. Hiroshima, and K. Mameno

Microelectronics Research Center, Sanyo Electric Co., Ltd.
180, Ohmori, Anpachi-cho, Anpachi-Gun, Gifu 503-0195, Japan
Phone: +81-584-64-5280, e-mail: hfujiwr@ul.rd.sanyo.co.jp

1. INTRODUCTION

We propose a new method for measuring the actual coupling coefficient of a split-gate Flash EEPROM whose floating gate voltage is controlled by the source voltage [1]. In contrast to previously proposed methods [2]-[6], ours adequately obtains the coupling coefficient of split-gate cells without the need for an additional test structure. In this method, the subthreshold current is measured twice as the source voltage is increased after the control gate transistor has sufficiently turned on. After the drain voltage is slightly altered (ΔV), the subthreshold curve is $\Delta V/\alpha$ shifted from the previous one. The coefficient α extracted in this work is in good agreement with that obtained by the conventional subthreshold slope method using the test structure. Analysis using device simulation also shows that our method can adequately obtain α.

2. EXPERIMENTAL

Figure 1 shows the split-gate Flash EEPROM for which we measure the coupling coefficients. The oxide thicknesses under the floating gate and control gate are 10 nm and 25 nm, respectively. Typical devices for measurement have a 0.75-μm channel width, 0.35-μm floating gate length and 0.4-μm control gate length. The threshold voltage of the control gate transistor is adjusted to 0.8 V. The source diffusion widely overlaps the floating gate's bottom, so that the coupling capacitance ratio between the source and the floating gate is large and the floating gate voltage is well controlled by regulating the source voltage.
The floating gate voltage, V_F is given by [3]

$$V_F=\alpha_S V_S+\alpha_C V_C+\alpha_B V_B+\alpha_D V_D+\frac{Q_F}{C_T} \quad (1)$$

Here, V_S, V_C, V_B, and V_D are the applied voltage to source, control gate, substrate, and drain, respectively; Q_F is the charge in the floating gate; $C_T=C_{SF}+C_{CF}+C_{BF}+C_{DF}$ is the sum of the source to floating gate capacitance (C_{SF}), the control gate to floating gate capacitance (C_{CF}), the substrate to floating gate capacitance (C_{BF}), and the drain to floating gate capacitance (C_{DF}); the coupling coefficients are defined as $\alpha_S= C_{SF}/C_T$, $\alpha_C= C_{CF}/C_T$, $\alpha_B= C_{BF}/C_T$, $\alpha_D= C_{DF}/C_T$, and $\alpha_S+\alpha_C+\alpha_B+\alpha_D=1$. The capacitance, C_{SF} is defined as $\partial Q_F/\partial V_S$, where ∂Q_F is the induced charge in the floating gate due to ∂V_S.

Figure 2 schematically shows the basic idea of our new method for extracting α_S. In this method, the subthreshold current beneath the floating gate must be evaluated as the source voltage is increased. The floating gate, therefore, must be written softly (negatively charged) so that the floating gate transistor may turn on after the control gate transistor has sufficiently turned on. The subthreshold current (I_S) can be modeled by [2]

$$I_S=I_0 \exp[\chi (V_F -V_T -\Delta V)] \quad (2)$$

where V_T is the threshold voltage of the floating gate transistor; and I_0, χ and ΔV are constants. After the drain voltage is increased by ΔV_D, the surface potential under the control gate is also raised by ΔV_D. The additional voltage of ΔV_D should thus be applied to the floating gate to achieve the same subthreshold current as before the drain voltage was altered. Consequently, an additional $\Delta V_D/\alpha_S$ of source voltage is necessary.

3. RESULTS AND DISCUSSION

Figure 3 shows the subthreshold current and the source voltage characteristics. Only the subthreshold current beneath the floating gate is evaluated to extract the source coupling coefficient. In the case of curve (a), the applied voltages V_C, V_B and V_D are 2.85 V, 0 V, and 1 V, respectively; V_S is increased from 1.0 V to 2.5 V. In the case of curve (b), V_D is 1.1 V; V_S is increased from 1.1 V to 2.5 V; other conditions are unchanged from (a). Identifying the source voltage for the same subthreshold current of 1×10^{-10}A in curves (a) and (b), the shift in the source voltage ΔV_S is 0.166 V. Since the V_F shift ΔV_F is equal to ΔV_D of 0.1 V, the source coupling coefficient is given by

$$\alpha_S = \Delta V_F/\Delta V_S = \Delta V_D/\Delta V_S = 0.602 \quad (3)$$

The value 0.602 is in good agreement with the coefficient 0.607 which is extracted by the conventional subthreshold slope method using a reference cell.

The simulated V_F and V_S characteristics are shown in figure 4 (curve (a)). The α_S is obtained by $\partial V_F/\partial V_S$, which is indicated as curve (b). The α_S is almost a constant value especially in the region where the V_S is roughly larger than 2 V. So the α_S extracted where the Vs is a little larger than 2 V takes almost the same value as that obtained around 10 V of the Vs. This means that the novel method can successfully extract the α_S of the write operation even though the Vs region for our measurement is smaller than the writing condition. The voltage difference between the source and the drain is less than 3 V during our entire measurement. This voltage condition is important for adequate measurement because additional electrons must not be injected into the floating gate during the measurement.

Figure 5 shows a device simulation of our new method. The coupling coefficient is obtained by

$$\alpha_S = \Delta V_D/\Delta V_S = 0.65$$

The extracted value is in good agreement with the value 0.68 estimated at V_S of about 10 V in figure 4.

4. CONCLUSION

We have presented a new method for measuring the coupling coefficients of an actual split-gate Flash EEPROM without an additional test structure where there is an electrical contact to the floating gate. This method can successfully extract the source coupling coefficient, which is in good agreement with that obtained by the previously reported subthreshold slope method and a device simulation.

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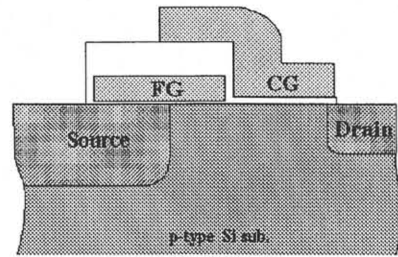

Fig. 1: Split-gate Flash EEPROM used in this work.

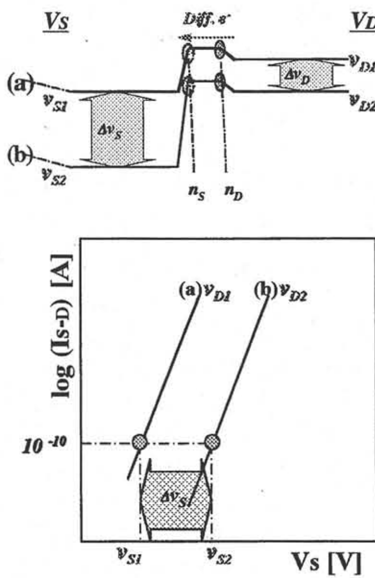

Fig. 2: Basic idea of our new method for extracting α_S.

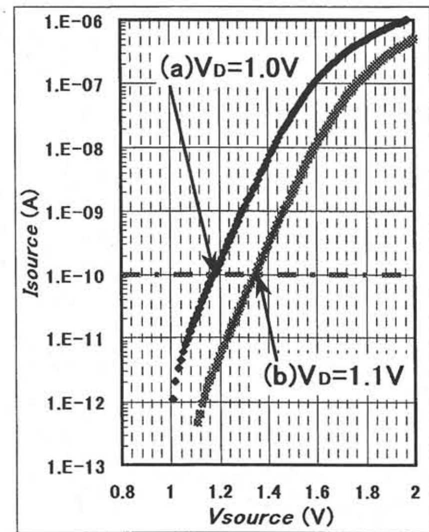

Fig. 3: Subthreshold current and source voltage. (a) V_C, V_B and V_D are 2.85 V, 0 V, and 1 V, respectively; V_S is increased from 1.0 V to 2.5 V. (b) V_D is 1.1V; V_S is increased from 1.1 V to 2.5 V; other conditions are unchanged from (a).

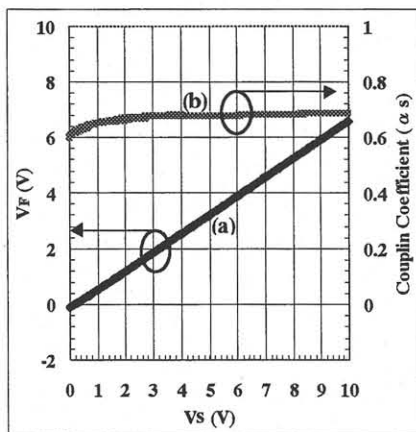

Fig. 4: Simulated V_F - V_S characteristics (a) and α_S (b).

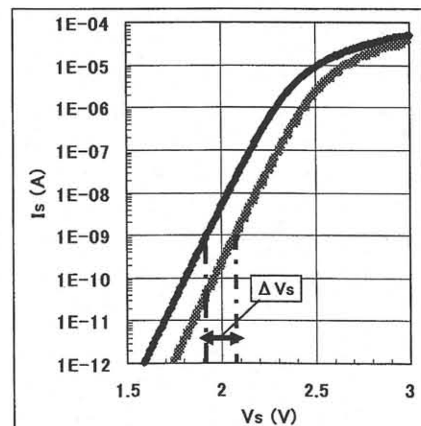

Fig. 5: Device simulation of our new method.