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A 2W High Efficiency 4-12 GHz GaAs HFET MMIC Power Amplifier

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1. Introduction

Microwave solid state high power amplifiers for use in phased array radar are required to be small and to achieve high gain, high power, and high efficiency over a wide bandwidth. As regards high power amplifiers employing GaAs PHEMT or HBT over 1.5-octave, several works of 1-1.8W output power levels, over 17% power-added efficiency, over 6-18 GHz[1-3], 4.5-16 GHz[4] and 4.5-18 GHz[5] have been reported. In the design of wideband lossy match power amplifiers employing GaAs PHEMT or HFET, we have proposed pre-matching circuits comprised of a short stub to make the frequency-dependence of FETs input impedance small[6], split-cell FETs layouts to achieve high gain[7], and a multisection maximally flat impedance transformer whose length is designed to become a quarter wavelength at the high frequency of the design band to achieve flat gain and flat power response[8].

In this paper, we describe design methods of an improved pre-matching circuit comprised of two short stubs and FETs layouts comprised of tapered power divider/combiner to achieve size reduction and high gain. With the use of these matching circuits, the amplifier employing GaAs HFET with 3 x 6 mm^2 has achieved a small signal gain of 15dB, a 2dB compressed power of 33dBm, and a power-added efficiency of 20-29% for CW operation over 4-12 GHz.

2. Power Amplifier Design

A schematic diagram of the improved pre-matching circuit comprised of two short stubs is shown in Fig.1. Two short stubs comprised of inductors L_1, L_2, resistors R_1, R_2 and a capacitor C_1 are directly connected to the gate terminal of FET represented with the gate-source capacitor C_{gs} and the inner resistor R_i. By representing L_1, R_1, L_2 with C_{gs}, R_i, C_1 and setting R_2 same as R_i, the frequency-dependence of Z_{in} (input impedance of FET with the pre-matching circuit) becomes small like as a conventional pre-matching circuit. Furthermore C_1 may be decided to achieve high gain of a FET.

A FETs layout comprised of tapered power divider/combiner is shown in Fig.2. Tapered divider and combiner are employed to two FETs. As no wilkinson dividers are used, divider size is reduced. Furthermore, by using divider with slits at the divider ports, high gain can be achieved.

A two stage power amplifier has been designed by optimizing parameters initialized by use the technique above-menthioned. A 1.4mm gate width FET in the first stage, and four 1.4mm gate width FETs in the second stage are used. The input matching circuit with the pre-matching circuit comprised of two short stubs and a impedance transformer is designed to reach an input return loss of about 2dB for balanced configuration and a gain to drive the second stage. The interstage and output matching circuits with conventional pre-matching circuits and impedance transformer are designed to reach an output return loss of about 10dB and an output power of 33dBm.

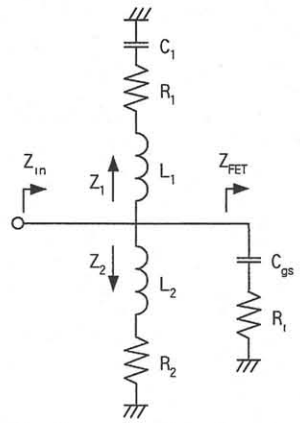

Fig. 1 A schematic diagram of the improved pre-matching circuit comprised of two short stubs.

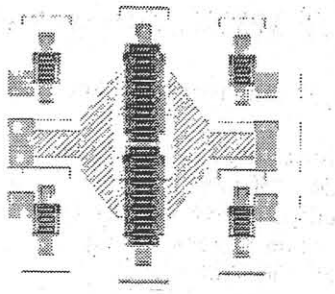

Fig. 2 A FETs layout comprised of tapered power divider/combiner

3. Fabrication and Performance

A photograph of the single-ended amplifier is shown in Fig.3. The amplifier was fabricated on GaAs substrates. The FETs used have a buried PHS structure to achieve low source inductance and good heat dissipation. The chip size is 3x6x0.1mm^3.

The measured results are shown in Figs.4 and 5. The bias conditions are V_d=9V and I_{ds}=1/5I_{dss}. For measurements, the chip was solded on to Cu-W carrier and mounted into a coaxial test jig, and the measured results are corrected for test jig losses. The small signal gain is 15dB, the input return loss is 2dB, the output return loss is 8dB, the 2dB compressed power is greater than 33dBm and the power-added efficiency is greater than 20% for CW operation over 4-12 GHz.

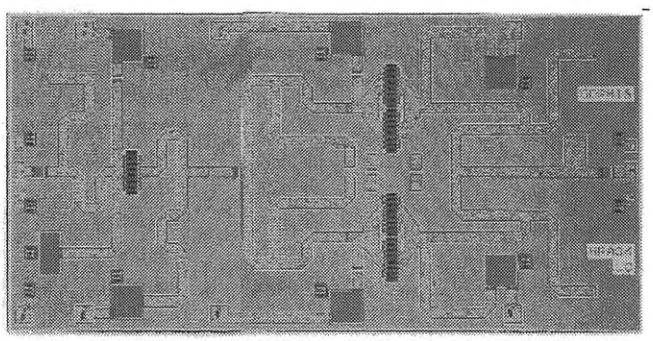

Fig. 3 A photograph of the single-ended amplifier.

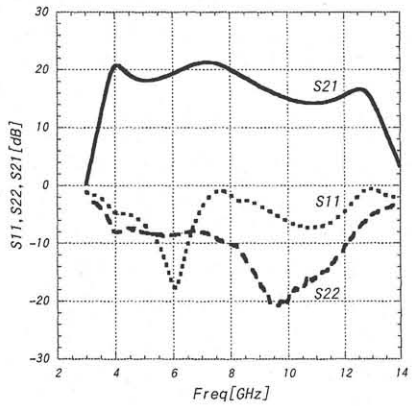

Fig. 4 The measured small signal gain and return losses.

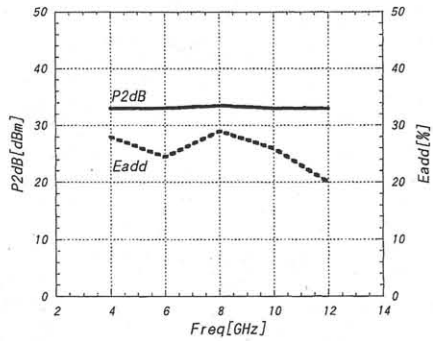

Fig. 5 The measured 2dB compressed power and power-added efficiency.

4. Conclusion

The design, fabrication, and performance of a 2W high efficiency 4-12 GHz GaAs HFET MMIC power amplifier have been presented. With the use of an improved pre-matching circuit comprised of two short stubs and FETs layouts comprised of tapered power divider/combiner, the amplifier with 3 x 6 mm^2 has achieved a small signal gain of 15dB, a 2dB compressed power of 2W, a power-added efficiency of 20-29% over 4-12 GHz.

References

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