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# Ku-Band Multi-Stage MMIC Low-Noise Amplifier Loaded with Double Gain-Equalizing Circuits

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## 1. Introduction

Multi-stage low-noise amplifiers employed in the active phased array receiver module for use in the mobile and satellite communication systems are required to show low noise figure, flat gain response, and small reflections for achieving small amplitude and phase tracking errors between modules. Large reflections of low-noise amplifiers produce gain and phase ripples of the receiver module, leading to serious amplitude and phase tracking errors between modules. To achieve low noise figure and small reflections simultaneously for multi-stage low-noise amplifiers, we have presented the design method to use source inductors with a different value for each stage FET [1]. The method was based on a narrow-band design and did not address the design issue how to achieve flat gain response over a wide bandwidth. To address this problem, two design techniques are employed: one is to use source inductors with a different value of FETs for achieving simultaneous noise and gain matching. The other is to use double gain-equalizing circuits in the design of interstage circuits for achieving flat gain response. The double gain-equalizing circuit, which has two resistors combined with short-circuited stubs, can provide a design flexibility to achieve an arbitrary gain equalizing. With the use of these two design techniques, a Ku-band three-stage MMIC low-noise amplifier has achieved an averaged gain of 33.5 dB, a gain flatness of 0.6 dB, input and output return losses of better than 10 dB, and a minimum noise figure of 1.2 dB over 11 to 12.5 GHz.

## 2. Device Performance

The 0.2 x 200 $\mu m^2$ AlGaAs/InGaAs/GaAs p-HEMTs without source inductors for use in the Ku-band low-noise amplifier were evaluated first by I-V measurements, S-parameters up to 40 GHz, and noise parameters at 12 GHz. The p-HEMT showed the minimum noise figure of 0.58 dB with an associated gain of 10.5 dB at 12 GHz for Vd = 2 V and Id = 17 mA. The small-signal and noise model parameters[2] were obtained from the measured S-parameters and noise parameters, which are summarized in Table 1.

Table I Noise model parameters of 0.2 x 200 $\mu m^2$ AlGaAs/InGaAs/GaAs p-HEMTs without source stubs and via holes

| | | | | | |
|---|---|---|---|---|---|
| gm | 107 mS | $C_{gs}$ | 0.17 pF | $F_{min}$ | 0.58 dB |
| $R_g$ | 5.2 Ω | $C_{dg}$ | 0.036 pF | $R_n$ | 9 Ω |
| $R_i$ | 1.5 Ω | $C_{ds}$ | 0.048pF | $\Gamma_{opt}$ | 0 49, 26 6 deg |
| $R_s$ | 0.2 Ω | $L_s$ | 0.01nH | $T_g$ | 300 deg |
| $R_d$ | 2.4 Ω | τ | 0.28 psec | $T_d$ | 1000 deg |
| $R_{ds}$ | 123 Ω | | | Freq. | 12 GHz |

## 3. Circuit Design

A schematic diagram of the Ku-band three-stage MMIC low-noise amplifier is shown in Fig. 1. It employs source inductors with a different value for each stage FET ($L_{S1}$, $L_{S2}$, and $L_{S3}$) to achieve simultaneous noise and gain matching of multi-stage low-noise amplifiers. In addition, the amplifier employs double gain-equalizing circuits in

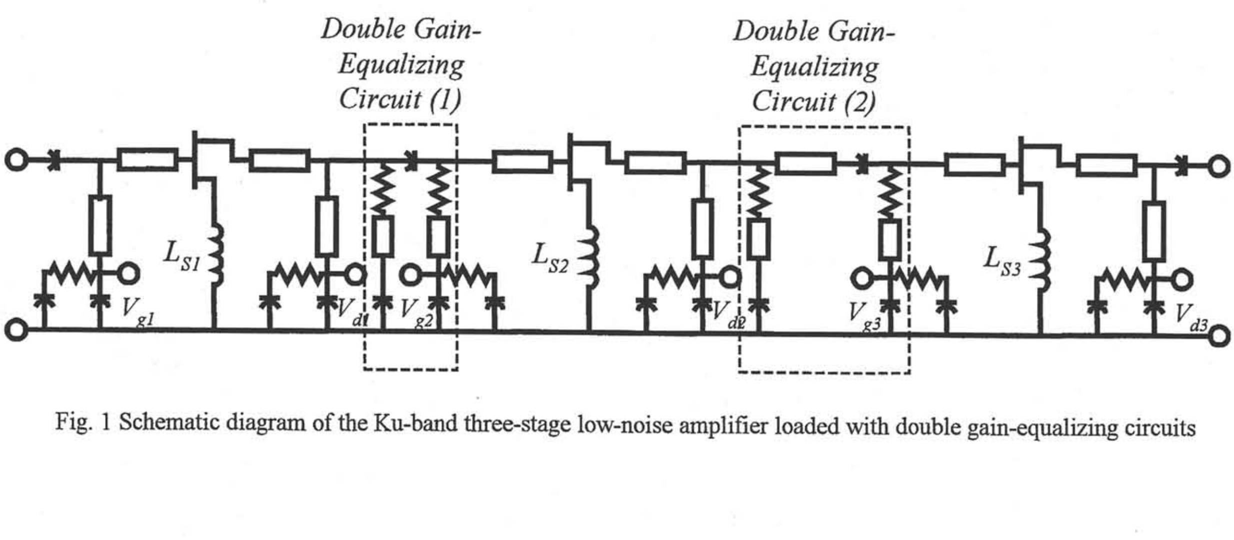


Fig. 1 Schematic diagram of the Ku-band three-stage low-noise amplifier loaded with double gain-equalizing circuits

the design of interstage circuits to achieve flat gain response over a wide bandwidth. A schematic diagram of the double gain-equalizing circuit is shown in Fig. 2. It is comprised of two resistors combined with short-circuited stubs. The values of resistors ($R_1$ and $R_2$) and stub lengths ($\theta_1$ and $\theta_2$) are designed to achieve flat gain response of the three-stage low-noise amplifier at Ku-band. In addition, the values of resistors ($R_1$ and $R_2$) of the double gain-equalizing circuit have to be carefully determined not to degrade noise figure performance. The reason why two resistors and short-circuited stubs are used is to provide design flexibility for required gain slopes. The d. c. decoupling capacitor (C) also plays an important role to share frequency-dependent gain equalizing performance between two gain-equalizing circuits. The double gain-equalizing circuits, which stabilize the circuit by using resistors, are employed only in the interstage circuits not to degrade noise figure or power performance. Except the double gain-equalizing circuits, a reactive matching is incorporated in the design of input noise matching and output gain matching circuits by using only series and shunt transmission lines. The gate and drain bias circuits include additional resistors and capacitors to remove low frequency oscillations.

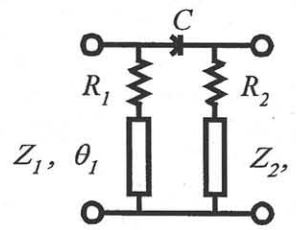


Fig. 2 Double gain-equalizing circuit

## 4. Circuit Fabrication and Performance

A photograph of the Ku-band three-stage MMIC low-noise amplifier loaded with double gain-equalizing circuits is shown in Fig. 3. The chip dimension is 2.0 x 3.5 x 0.1 $mm^3$. d. c. and r. f. performances were evaluated by using the on-wafer prober. The calculated and measured noise figures, gains, and return losses are plotted in Fig. 4. The amplifier showed an averaged gain of 33.5 dB, a gain flatness of 0.6 dB, input and output return losses of better than 10 dB, and a minimum noise figure of 1.2 dB over 11 to 12.5 GHz. The calculated and measured results are basically in good agreement. A slight discrepancy appears for the output return loss. This is most likely due to some errors in the modeling of the p-HEMT. In addition, the measured noise figure becomes worse below 11.5 GHz. This is probably due to the measurement errors of the on-wafer testing systems. The bias conditions are Vd = 2 V and Id = 50 mA.

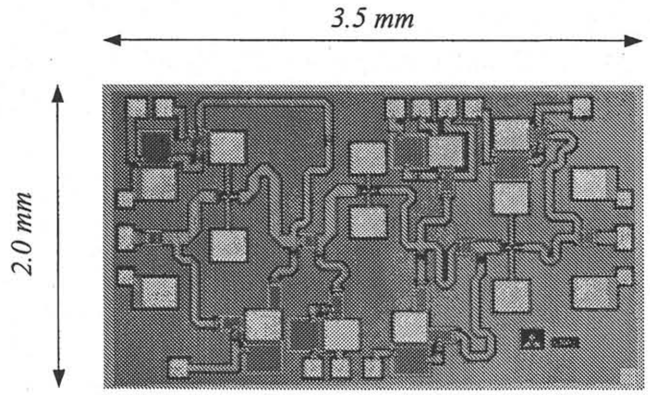


Fig. 3 Photograph of the Ku-band three-stage low-noise amplifier loaded with double gain-equalizing circuits

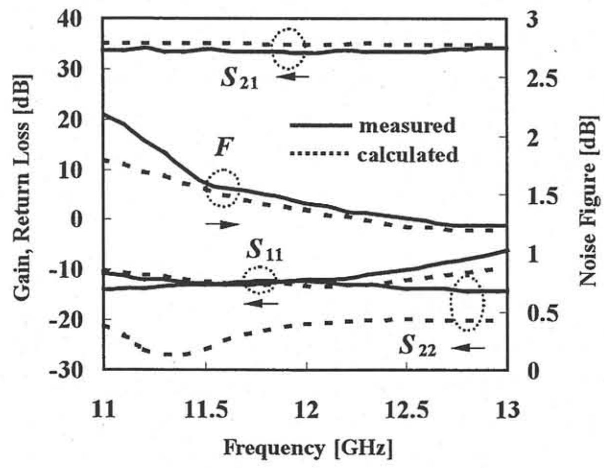


Fig. 4 Calculated and measured noise figures, gains, and return losses of the Ku-band three-stage low-noise amplifier loaded with double gain-equalizing circuits.

## 5. Conclusions

A Ku-band three-stage MMIC low-noise amplifier using double gain-equalizing circuits has been developed for use in the active phased array receiver module. The three-stage MMIC low-noise amplifier with 0.2 x 200 $\mu m^2$ AlGaAs/InGaAs/GaAs p-HEMTs has achieved an averaged gain of 33.5 dB, a gain flatness of 0.6 dB, input and output return losses of better than 10 dB, and a minimum noise figure of 1.2 dB over 11 to 12.5 GHz with the use of the double gain-equalizing circuits and source inductors with a different value for each stage FET.

## References


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