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Future SOI Technology and Devices

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1. Introduction

This paper reviews SOI MOSFET structures for future deep sub-100nm and low-voltage, low-power VLSI applications.

2. SOI Materials

For a long time SOI technology was considered unpractical for mainstream commercial applications because of the poor quality of the material and the limited throughput of SOI wafer manufacturers. These hurdles are now a thing of the past due to the improvements of SIMOX technology (high-quality, low-dose material) and the advent of the SmartCut® process.

3. Basic SOI MOSFET structures

FD and PD MOSFETs

Traditionally SOI MOSFETs have been classified into two families: partially depleted (PD) devices and fully depletd (FD) devices. In PD SOI MOSFETs the threshold voltage is independent on silicon film and BOX thickness variations, but numerous floating-body effects may render the use and the simulation of the device difficult or unreliable. In FD SOI MOSFETs the floating-body effects are much reduced but V_{TH} depends on silicon film thickness, even though this does not seem to be a problem with recent SOI materials where film thickness control is excellent. FD MOSFETs have a low body effect coefficient (n=1.05...1.1 compared to n=...1.5 in bulk), which gives them excellent current drive and subthreshold characteristics. A body effect coefficient close to unity can be obtained using multiple-gate and merged bipolar-MOS SOI structures.

4. Novel SOI MOSFET structures

Like any MOSFETs, SOI devices see their behavior deviate from ideal "long-channel" characteristics in the deep-submicron regime. This is mostly due to the encroachment of electric field lined from the drain on the body of the device (between source and drain). Several device structures aim at correcting this problem and are discussed next.

Ground-Plane SOI MOSFET

To keep electric field lines from the drain from propagating into the channel region a ground-plane can be formed in the silicon substrate underneath the buried oxide.[1,2] A heavily doped electric-field stop can be placed in the substrate either underneath the boundary between channel and source/drain or underneath the channel region itself (Figure 1). This field stop effectively improves short-channel effects and subthreshold slope.

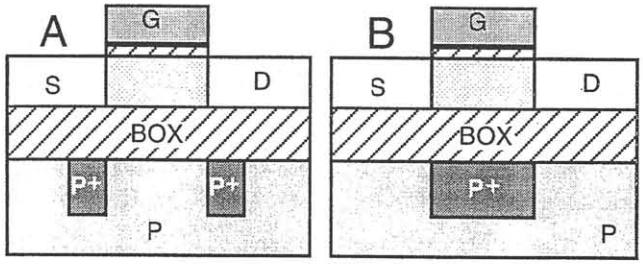

Fig. 1: Ground-plane under A) source and drain edge [3] or B) channel region [4].

"Multiple-gate" SOI MOSFET

To keep electric field lines from the drain from encroaching on the channel region special gate structures can be used (Figure 2). Such "multiple"-gate devices include double-gate transistors, triple-gate devices such as the quantum wire [5], the FinFET [6] and Δ-channel SOI MOSFET [7], and quadruple-gate devices such as the gate-all-around device [8], the DELTA transistor [9], and vertical pillar MOSFETs [10,11].

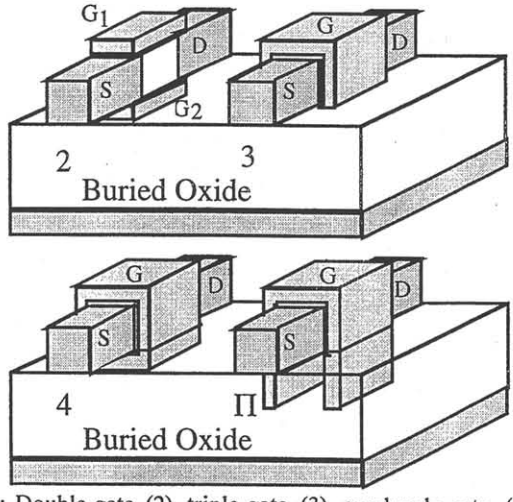

Fig. 2: Double-gate (2), triple-gate (3), quadruple-gate (4) and Π-gate MOSFET (Π) [12].

The more the gate surrounds the channel region the better the shielding from the drain. Quadruple-gate devices are difficult to fabricate, but the Π-gate structure can be readily manufactured and offers characteristics close to those of a quadruple-gate MOSFET (Figures 3 and 4).

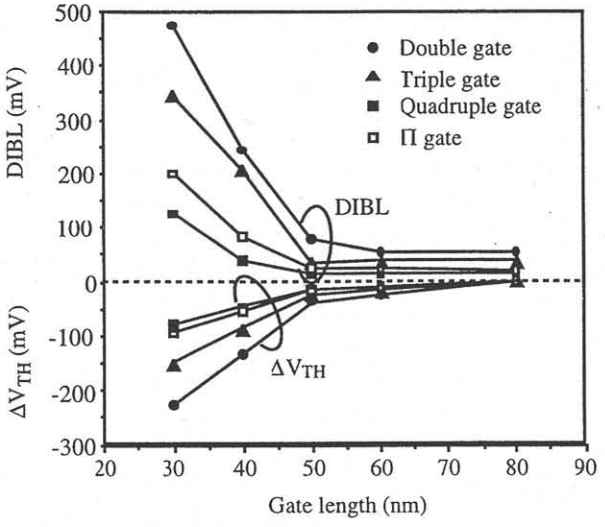

Fig. 3: V_{TH} roll-off and DIBL in double, triple, quadruple and Π-gate SOI MOSFETs. Device width and thickness = 30 nm.

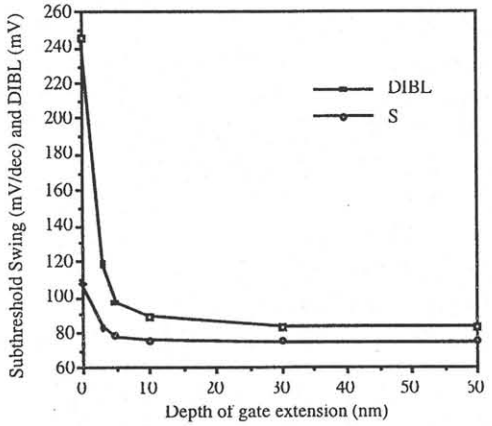

Fig. 4: DIBL and S in Π-gate SOI MOSFETs. vs. depth of gate extension in BOX. Device width = t_{si} = 30 nm, L = 40 nm.

Compared to single-gate MOSFETs multiple-gate MOSFETs of small dimensions offer a more symmetrical distribution of carrier wavefunctions in the silicon, which yields an improved mobility and volume inversion effects.[5,13,14]

Novel junction structures for SOI MOSFET

To reduce source and drain resistance in thin-film SOI devices the use Schottky junctions [15,16] or metal junctions with tunnel barriers [17] junctions may become mandatory.

5. SOI Circuit Applications

It seems that SOI technology is particularly suited for low-power, low-voltage (0.5-0.9V) applications, where its high I_{ON}/I_{OFF} ratio is a decisive asset. The merged bipolar-MOS SOI transistor [18,19] (also called DTMOS or MTCMOS) offers a body effect coefficient equal to unity and is, therefore, a good contender for such applications, although contacting the channel region might not be a practical solution in very short-channel devices.

6. Conclusion

SOI device structures for deep sub-100nm technology nodes are proposed. DIBL and other short-channel effects can be reduced through e-field shielding structures. SOI seems well adapted to future low-power VLSI electronics needs.

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