Novel Fabrication Technique for Relaxed SiGe-on-Insulator Substrates
without Thick SiGe Buffer Structures

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1. Introduction
Strained-Si MOSFETS are one of the most promising device structures for high speed sub-100-nm CMOS [1]. Furthermore, we have recently proposed fully-depleted strained-SOI (strained-Si-on-Insulator) MOSFETS fabricated on relaxed SiGe-on-insulator (SGOI) films [2]. To form a strained-Si channel on relaxed SiGe layer, a thick SiGe buffer layer is a key technology for the lattice relaxation of the top SiGe layer, as shown in Fig.1 (1). Combining this thick SiGe buffer structure with the SIMOX technology (Fig.1 (2)), strained-SOI n- and p-MOSFETS with the enhancement of electron (60%) and hole (30%) mobility have been demonstrated [2]. In order to further improve the device performance, on the other hand, the increase in the Ge content of SGOI and much thinner SGOI films are mandatory. However, there are mainly two problems to realize such SGOI substrates, as described below.

Problem-1: Their large drain leak current is attributable to the dislocations in top SiGe layer. High density of dislocations is still induced by thick SiGe buffer structure [3]. Therefore, it is necessary to develop a new technology for realizing relaxed SGOI layers compatible with low dislocation density.

Problem-2: The melting point of SiGe layers with high Ge content is too low for high temperature annealing in the SIMOX process [3], [4]. As shown in Fig.2, it is found that, when SIMOX annealing at 7-1350°C was carried out for SiGe layers with the Ge content of 20%, a continuous buried oxide layer is not fabricated and only some oxide islands are formed, whereas a buried oxide layer is successfully formed for the Ge content of 10% [2]. This failure of uniform buried oxide formation is attributed to the out-gas of implanted oxygen atoms from the SiGe layer, because the SIMOX annealing temperature is higher than the melting point of SiGe layer with Ge content of 20% [5]. Since the lower limit for SIMOX annealing temperature is around 1320°C, the Ge content is also limited to be lower than 14% [4].

In this work, we propose a novel technology for high-quality relaxed SGOI substrates without using thick SiGe buffer layers. At first, in order to avoid the problem-1, a thin strained-SiGe structure, pseudomorphically grown on Si substrates, with no graded SiGe buffer layer and low Ge content is used for a starting substrate for the SIMOX process. To overcome the problem-2 and to increase the Ge content, low temperature ITOX [6] process is added to the SIMOX annealing, resulting in the increase of the Ge content by thinning SGOI substrates [7] after the SIMOX process.

II. Novel Fabrication Process for SGOI structures
Fig.3 shows the new process for relaxed SGOI structures with higher Ge content. As shown in Fig.3(1), a 300-nm-thick strained Si$_{1-x}$Ge$_x$ film was formed directly on a Si substrate without thick graded SiGe buffer structures. This thickness should be much thinner than the critical thickness of SiGe on Si [8] at growth temperature of the SiGe epitaxy, in order to suppress the dislocation generation in this SiGe layer. Next, as shown in Fig.3(2), the SIMOX process (oxygen ions dose of 4x10$^{12}$ cm$^{-2}$) was carried out to form the buried oxide between the top SiGe and the Si substrate, leading to the relaxation of the strained SiGe layer through a slip between the top SiGe and the buried oxide. The sufficiently low Ge content allows using the SIMOX annealing at high temperature of 1335°C, which is necessary to form a continuous buried oxide layer. After that, that SGOI was thinned by low temperature ITOX process [6] (annealing in Ar-O$_2$ mixture gas) to increase the Ge content, as indicated in Fig.3 (3). Here, this annealing temperature (1200°C) should be lower than the melting point of SiGe layer. When SiGe layers are oxidized, Ge atoms are rejected from the oxide. On the other hand, the diffusion of the Ge atoms toward substrates is blocked by buried oxides, resulting in condensing into the remaining SGOI layers [7].

III. Results and Discussions
As shown in SEM observation of dislocations in top SiGe layer in Figs.4 (b) and (c), the dislocation density of SGOI without SiGe buffer layer can be reduced by about one order of magnitude, compared to that with thick and relaxed SiGe buffer layer. Figs.4 (a) and (b) also show that the dislocation density of SGOI substrate are about one third of that of bulk SiGe before SIMOX process, suggesting that the dislocation density of SiGe layer can also be reduced by high temperature SIMOX annealing.

Fig.5 shows the TEM photographs of the cross section of the SGOI substrates after (a) SIMOX and (b) ITOX processes. It is confirmed that the buried oxide is uniformly fabricated by the SIMOX process. After the ITOX process, the SiGe thickness on the buried oxide is thinned to 40 nm from 300 nm, which is effective in suppressing short channel effects of MOSFETS. It is also observed that the buried oxide thickness increases from 80 nm to 110 nm. Thus, the improvement in the breakdown voltage of the buried oxide is expected in this SGOI substrate after the ITOX process.

Fig.6 shows the Ge content profile of SGOI substrate, evaluated by Auger electron spectroscopy. After SIMOX process, the Ge content (thin line) becomes uniform (about 3.6%) and is about one third of the initial Ge content (dashed line) in whole SiGe layer on the buried oxide, because Ge atoms diffuse toward the Si substrate during the high temperature annealing process. However, after ITOX process (bold line), the Ge atoms are condensed to 20% from 3.6%, because Ge atoms are rejected into the remaining SiGe layer during thinning process due to oxidation [7]. These results means that the combination of SIMOX and ITOX processes enable to obtain SGOI with the Ge content higher than in the initial strained SiGe layer.

Fig.7 shows the Raman shift (circles) $\Delta \omega$ of SGOI after SIMOX ($\times$3.6%) and ITOX ($\times$20%) processes and the relaxation rate (triangles) as a function of the Ge content $x$ of SGOI substrates. The relaxation rate is defined by $(\Delta \omega / \Delta \omega_{\text{bulk}}) / (\Delta \omega_{\text{relax}} / \Delta \omega_{\text{bulk}})$, where $\Delta \omega_{\text{bulk}}$ and $\Delta \omega_{\text{bulk}}$ are the calculated Raman shifts of fully strained and relaxed SiGe layers [9], respectively. The SGOI substrate from a thin and strained SiGe layer is fully relaxed after the SIMOX process. This SGOI substrate is almost fully relaxed (93%) even after the low temperature ITOX process. The relaxation of the SGOI substrate is ascribed to large slip between the top SiGe layer and the buried oxide.

IV. Conclusion
We have developed the novel technology for relaxing top
SiGe layers on Si substrates, without using thick SiGe buffer layers. By newly introducing a thin strained SiGe layer and the ITOX process following the SIMOX process, relaxed SGOI substrates with the Ge content of 20% and the dislocation density of one order of magnitude lower than in previous ones have been experimentally demonstrated. This SGOI substrate is applicable to high-speed strained-SOI MOSFETs under sub-100-nm regime.

References