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Thinner SOI Using Plasma Hydrogenation

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1. Abstract

We describe for the first time blistering of a silicon surface upon thermal annealing following DC plasma hydrogenation. The process involves first making a buried trap layer using variously argon, helium, or hydrogen implantation. Wafers thus processed with an initial implant to levels below $4x10^{16}$ cm^{-2} are then hydrogenated with a DC plasma. Following thermal annealing, blistering occurs with a depth corresponding to the maximum of vacancy-enriched defects (about $R_p/2$) for the lowest implant doses and up to R_p for the high implant doses. This process may be used as a step in the process of fabricating thin SOI wafers.

2. Introduction

The International Technology Roadmap for Semiconductor Technology [1] projects that the top silicon layer for SOI starting wafers will be 20 to 100 nm in thickness by 2004 to support processing of fully-depleted CMOS circuits. At the present time processes such as Smart-Cut™ provide a minimum silicon film thickness of about 200 nm [2]. The thickness of the delaminated layer in the Smart-Cut process depends on the energy of implantation of hydrogen. When the energy of the hydrogen implant is reduced to levels below 50 keV to achieve thin delaminating thickness problems arise. These problems include amorphization of the silicon surface or the Si-SiO_2 interface so the Smart-Cut process fails. Attempts have been reported to thin the surface silicon layer subsequent to hydrogen implantation in an effort to obtain SOI wafers with surface films of less than 200 nm thickness. Srikrishnan [3] forms an etch stop by implantation in to the top silicon layer with a subsequent etchback. Popov [4] reports a layer-by-layer oxidation with subsequent stripping in diluted HF for thinning of the layer. Both approaches increase SOI wafer production cost and decrease thickness uniformity. Our work here reports the utilization of DC plasma hydrogenation as a post process following a low level implant to create the desired surface layer of thickness less than 100 nm.

3. Experimental

Silicon wafers were ion implanted with either argon, helium or hydrogen to form buried trap layer for hydrogen. Then the as-implanted wafers were hydrogenated in DC plasma setup described in [5] under conditions listed in the Table 1. In some cases then the wafers were annealed at 450°C. Depending from the implantation dose, parameters of the hydrogen plasma treatment and post-hydrogenation heat treatment the wafer surfaces show blistering. The wafers were then angle lapped (beveled) to reveal the blister depth. The blister depths were analyzed with optical microscope and profilometry. The samples were also analyzed by SEM and Raman measurements.

4. Results

The wafer surface after annealing shows a typical "blistered" shape, similar to that obtained after high dose (over $4x10^{16}$ cm^{-2}) hydrogen implantation. Fig.1 and Fig. 2 show depths of the blisters measured with profilometry. Fig.3 and Fig.4 show x400 view of a beveled edge of the blistered wafers. Figs.1,3 shows revealed blisters on low dose $1x10^{16}$ cm^{-2} implanted wafer. Figs.2,4 show similar view of high dose ($4x10^{16}$ cm^{-2}) implanted wafer. H_2^+ was implanted in both cases. The "high" dose is close but lower, than a dose needed to blister the wafer without an additional hydrogenation. Similar pictures are obtained for cases of helium and argon implantation. For helium implantation the blisters are about x2 shallower, and for argon implantation the blisters are more than x10 shallower.

5. Discussion

Our previous work [6] shows silicon flaking along a hydrogenated trap layer. We used electrolytic hydrogenation. Next we tried to move from flaking to layer transferring. We found that the electrolytically hydrogenated wafers are hard to bond to a stiffener wafer for unknown yet reason.

An inherent delaminating thickness for either Smart-cut or the trap-filling processes are controlled by an implantation depths. For the Smart-cut the depth is the R_p of hydrogen while for the trap-filling process is between $R_p/2$ and R_p of heavier ions. Correspondingly, the layer transfer depths are 200-2000 nm, and 20-200 nm. Therefore, the trap-filling process is advantageable for making thin SOI.

As a example, pictures Figs.1-4 confirm featurability of DC plasma hydrogenation for SOI process based on traps-filling, which was provided as shown in Table. The pictures also show an important difference the delaminating depths, that are R_p and less than R_p for the Smart-Cut and trap-filling processes correspondingly. The pictures are shown for case of hydrogen, and the similar results are obtained for heavier ions (helium and argon), that are scaled for much deeper submicron range.

6. Conclusion:

DC plasma hydrogenation of a buried trap layer formed with heavy ion implantation can be used to develop a thin top Si SOI wafer process. An inherent top layer thickness is ~10 times lower than for a convenient Smart-Cut™ process.

Acknowledgements:
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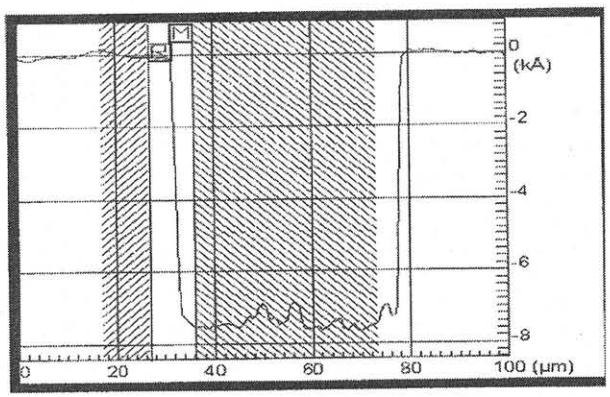


Fig.1 Depths of blisters revealed on high dose $4x10^{16}$ cm^{-2} implanted and DC plasma hydrogenated wafer (profilometry)

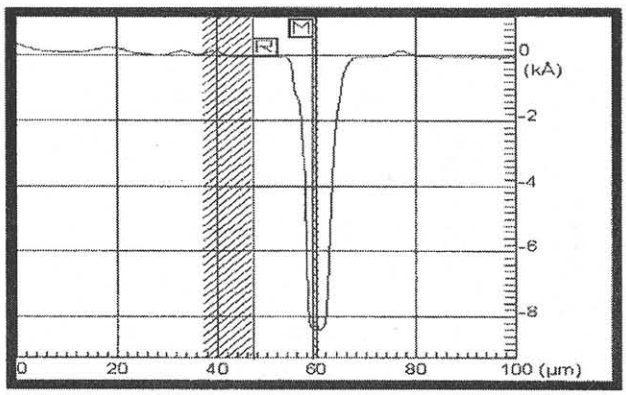
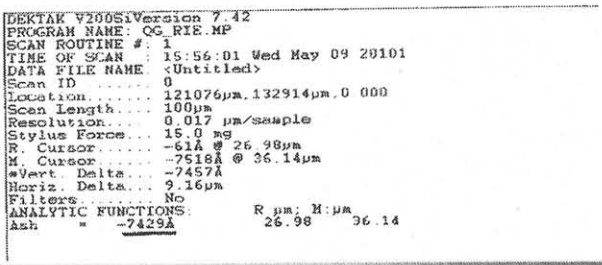


Fig.2 Depths of blisters revealed on high dose $4x10^{16}$ cm^{-2} implanted and DC plasma hydrogenated wafer (profilometry).



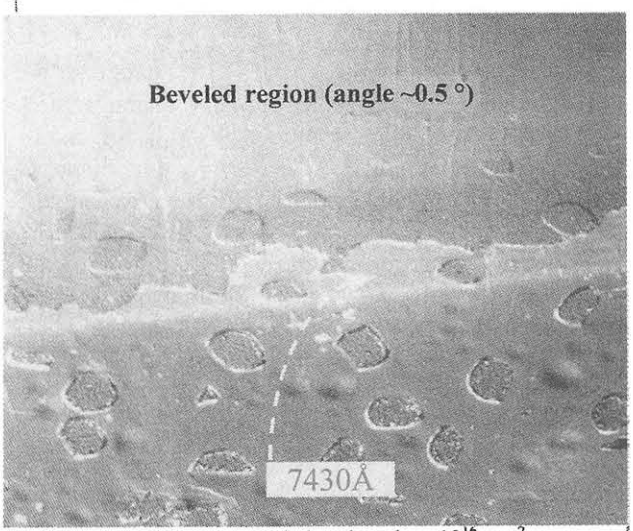
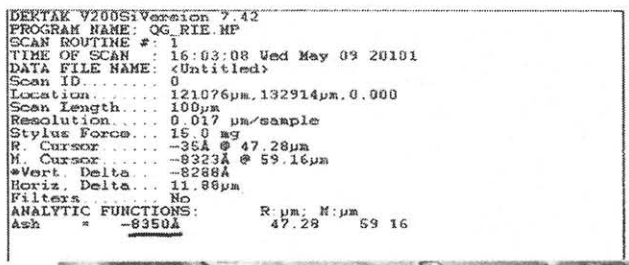


Fig.3 Depths of blisters revealed on low dose 10^{16} cm^{-2} implanted and DC plasma hydrogenated wafer (x400).



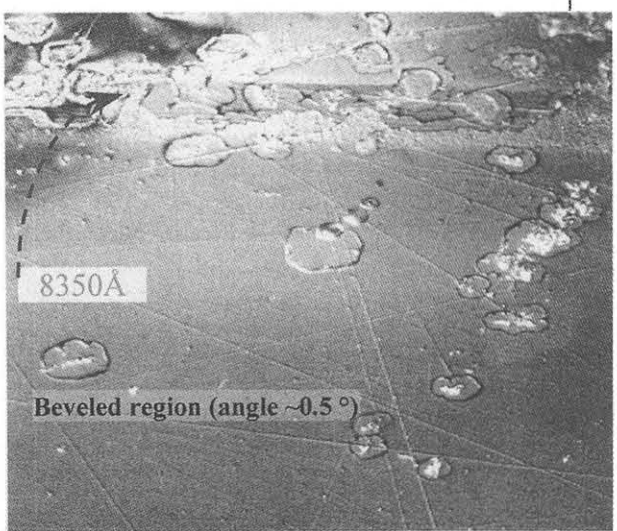


Fig.4 Depths of blisters revealed on high dose $4x10^{16}$ cm^{-2} implanted and DC plasma hydrogenated wafer (x400).

Table

	Wafer			Implantation		DC plasma		
	type	dopant	Resistivity	energy	dose	energy	Time	T°
Sample Fig.1, 3	P	Boron	1 Ohmxcm	100 keV	1x10E16	0 to 2 keV	1 hour	350°C
Sample Fig.2, 4	P	Boron	1 Ohmxcm	100 keV	4x10E16	0 to 2 keV	1 hour	350°C