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New SOI Flash Memory with Side Channel and Side Floating Gate

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Introduction

The integration density in electronics is increasing in breath-taking pace towards the Gbit generation despite all predictions about technological and physical limits. Nevertheless, principal physical limitations are unavoidable. Basically, the conventional devices need a charging energy more than single electron devices because of its large number of charges. In contrast, the single electron devices make use of the smallest unit of electric charge in order to represent bits of information. In addition, its current is controlled by a single electron. It has the potential of dramatic improvement in power consumption and packing density. However, the single electron devices have the drawback of low current drivability. Therefore, the small size devices which operate with several electrons are preferable. Then, we propose a new SOI Flash memory with side channel and side floating gate as a typical example of these devices which operate with several electrons.

A New SOI Flash Memory with Side Channel and Side Floating Gate

Figure 1 shows the schematic diagram of process flow for the new SOI Flash memory with side channel and side floating gate. In this Flash memory device, the side channel and side floating gate are used to reduce the floating gate area and then to decrease the number of electrons in the floating gate. The channel is formed at the side surface of very thin SOI film. The SOI film thickness is around 50nm. A floating gate covers the side channel. The channel width could be reduced to 30nm by using the side channel type device. The control gate is fabricated over the side channel.

Atomic layer doping technology

It is very difficult to dope the impurity into the side surface of SOI region using the conventional ion implantation. Then, we have developed a new atomic layer doping method. This atomic layer doping method is also used to dope the boron atoms into the top surface in SOI region to eliminate the parasitic channel since the boron should be doped in the very shallow surface region. Atomic layer doping was performed by using UHV-CVD apparatus. Boron of 3×10^{18}ions/cm^3 was adsorbed on the surface of SOI film in order to prevent the formation of a parasitic channel in the top surface. Figure 2 shows the boron impurity profiles obtained using atomic layer doping method. Atomic layer doping was also used to form the source and drain extension region in the side surface of SOI region. Arsenic was adsorbed the source and drain at the side surface because the source and drain cannot be formed at the side surface by using the conventional ion implantation method. Figure 3 shows the As impurity profiles obtained using atomic layer doping method.

Device Characteristics of SOI Flash Memory with Side Channel and Side Floating Gate

Figure 4 shows the SEM cross section of fabricated SOI Flash memory with side channel and side floating gate. In this device, the channel width and the floating gate width are determined by the SOI film thickness with boron undoped and the height of undoped amorphous silicon side wall which acts as a floating gate, respectively. The resistance of diffusion layer formed at the side surface which is used as the source and drain extension region is plotted versus the diffusion layer length. From this result, a sheet resistance of 3.4kΩ/□ was obtained for the source and drain extension region formed at the side region. Drain current-voltage characteristics of SOI Flash memory transistor with side channel and side floating gate are shown in Fig.6. The drain current does not change as the top width of SOI region is changed as shown in Fig. 7. Therefore, we confirmed that the drain current-voltage characteristics shown in Fig.6 are obtained for the SOI Flash memory transistor formed at the side of SOI region. Figure 8 shows the ID-VG characteristics of this device. The gate voltage is swept from -5V to 5V and back again. The devices show a clear hysteresis with a significant threshold voltage shift. The programming and erasing characteristics as a function of time are shown in Fig. 9.

Conclusions

A new SOI Flash memory with side channel and side floating gate has been proposed to reduce the power consumption and to increase the packing density. This device has the potential that it is operated with several electrons. A new atomic layer method is used to dope arsenic atoms into the side surface of SOI film for the formation of source and drain extension region and to dope boron atoms into the top surface of SOI region for the parasitic channel cut. The devices with the gate length of 0.1 μ m fabricated showed excellent characteristics.

Reference: Y. H. Song, H. Kurino, M. Koyanagi et al., IEDM, p.505 (1999).

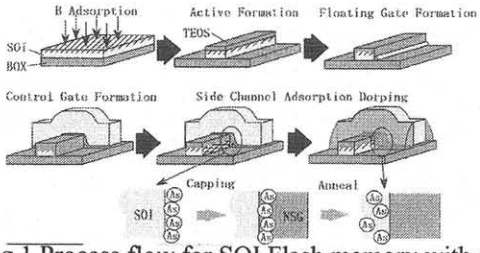

Fig.1 Process flow for SOI Flash memory with side channel and side floating gate using As atomic layer doping method

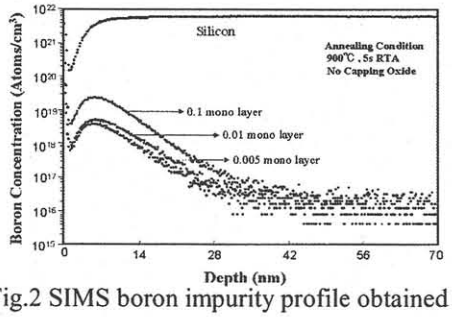

Fig.2 SIMS boron impurity profile obtained by atomic layer doping method

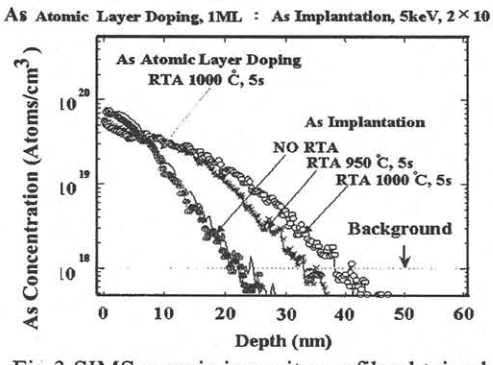

Fig.3 SIMS arsenic impurity profile obtained by atomic layer doping method

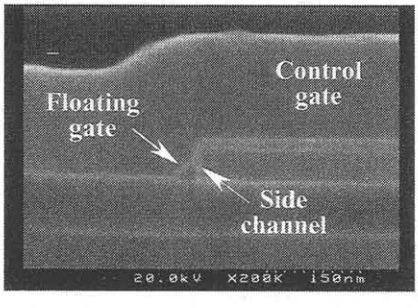

Fig.4 SEM cross section of SOI Flash memory with side channel and side floating gate

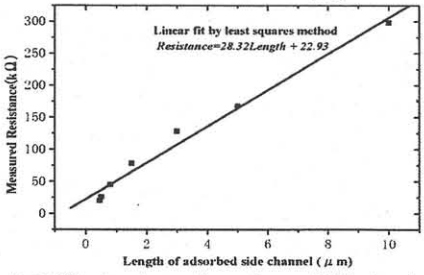

Fig.5 Diffusion layer length vs. diffusion layer resistance formed at the side of SOI region

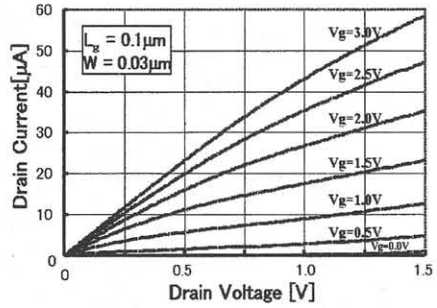

Fig.6 ID-VD characteristics of SOI Flash memory transistor with side channel and side floating gate

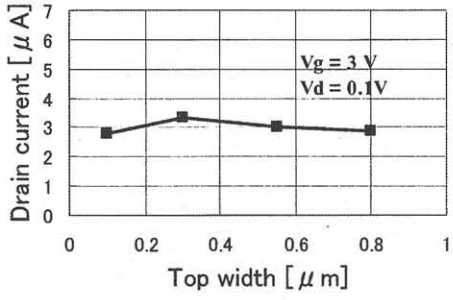

Fig.7 Isolation width dependence of drain current

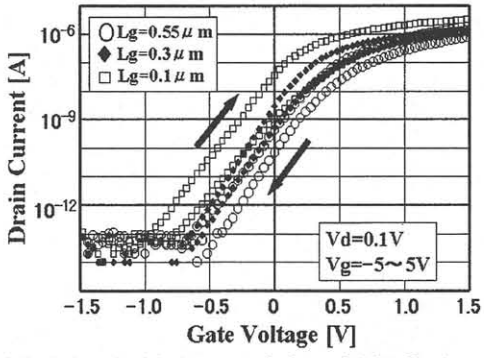

Fig.8 Subthreshold characteristics of SOI flash memory with side channel and side floating gate

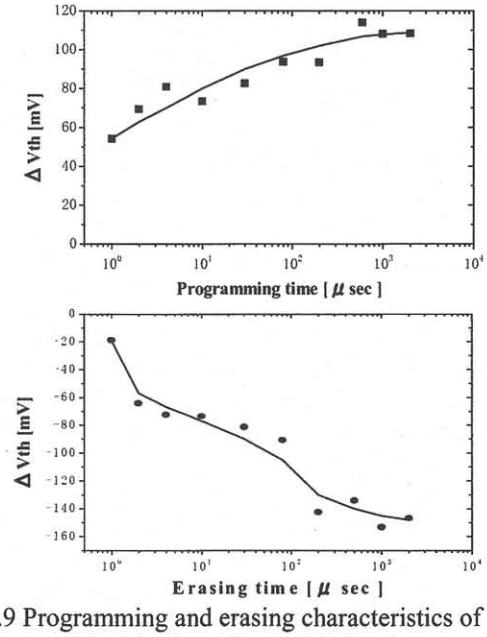

Fig.9 Programming and erasing characteristics of SOI Flash memory with side channel and side floating gate