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The Influence of the Device Miniaturization on the I_{on} Enhancement in the Intrinsic Silicon Body (*i-body*) SOI-MOSFET's

Risho Koh, Hisashi Takemura, Kiyoshi Takeuchi and Tohru Mogami

Silicon Systems Research Laboratories, NEC Corporation
Shimokuzawa 1120, Sagamihara, Kanagawa, 229-1198, Japan
phone:+81- 42-779-6193, Fax: +81-42-771-0886, E-mail: r-koh@ah.jp.nec.com

1.Introduction An SOI-MOSFET with intrinsic Si body (*i-body*) has a very attractive feature that a small effective vertical electric field (E_{eff}) enhances the carrier mobility (μ)[1]. However, it is not clear whether the device miniaturization[2], in which the device parameters such as the gate length (L), the supplied voltage (V_{DD}) and the gate oxide thickness (T_{OX}) are scaled down, enhances or reduces the advantage. Therefore, a systematical simulation is performed for device generations from L=0.25 to 0.05 μ m. It was found that μ enhancement and ON current (I_{ON}) enhancement in *i-body* SOI-MOSFETs become significant as the device generation advances (e.g., 38% I_{ON} improvement for L=0.25 μ m and 55% for 0.1 μ m, for a low power device), since the device has an ability to suppress E_{eff} which increases in a small bulk MOSFET.

2.Simulation Single gate and double gate *i-body* SOI-MOSFETs are assumed, and a uniformly doped Bulk MOSFETs as well (Fig.1). The threshold voltages (V_{th}) of *i-body* device are controlled by the work function of gate electrode. T_{SOI} and T_{BOX} (see Fig.1) are fixed at 10nm and 80nm, respectively. The device generation is represented by the MPU gate length L (Table.1). V_{DD} and T_{OX} are determined after ITRS[2] and SIA[3] roadmap. The OFF current (I_{OFF}) for low power device (L-type) is 3 orders of magnitude smaller than that of high performance device (H-type). The typical wire length for each generation is determined after[4]. Since a drift and diffusion 2D simulator used here can not model the velocity overshoot which is significant in n-channel devices, p-channel devices are mainly discussed.

3. μ and I_{ON} Figure 2 shows the position dependence of μ for p-channel devices, which is a function of the low field mobility μ_{eff} [5] and the horizontal field. It is evident that the μ enhancement in *i-body* SOI-MOSFETs becomes remarkable as the devices are miniaturized. Since it is known that an increase in effective vertical electric filed (E_{eff}) degrades μ_{eff} [5], E_{eff} is calculated as shown in Fig.3. The results show that E_{eff} increases only in the bulk MOSFETs when the generation advances. Therefore, E_{eff} reduction in *i-body* device becomes remarkable as the devices are miniaturized. This leads to the enhancement in μ_{eff} (Fig.4), I_{ON} and μ (Figs. 5 and 6) in a small *i-body* device.

The I_{ON} enhancement in H-type devices almost follows that of μ (Fig.6), with the exception of 0.08 μ m single gate device "(i)" which is affected by the short channel effect (a similar degradation appears in L-type). I_{ON} enhancement in L-type devices is much larger. One reason is that the E_{eff} reduction is more remarkable, since higher V_{th} increases the E_{eff} of bulk devices and low inversion charge density is efficient for decreasing E_{eff} of *i-body* devices. An additional effect which is attributed to the S factor improvement and a horizontal field enhancement due the SOI structure, is also significant in the L-type devices ("(ii)" in the figure).

4.Discussions on the μ enhancement E_{eff} in p-channel bulk device is given by

$$E_{eff} = qN_s / 3\varepsilon_{Si}\varepsilon_0 + qN_{dpl} / \varepsilon_{Si}\varepsilon_0 \quad (1)$$

where, q is the elementary charge, N_{dpl} is the depletion charge area density, N_s is inversion charge area density, ε_{Si} is dielectric constant of Si and ε_0 is that of vacuum. By substituting usual equation on V_{th} for eq.(1), one obtains

$$E_{eff} = qN_s / 3\varepsilon_{Si}\varepsilon_0 + q(V_{th} - \Phi_{ms} - 2\Phi_F)\varepsilon_{OX} / \varepsilon_{Si} T_{ox} \quad (2)$$

where, ϕ_{ms} is the work function difference between gate and source, ϕ_F is the Fermi potential. Through the miniaturization, a large variation in T_{OX} is required to achieve appropriate I_{ON}, however, in order to suppress I_{OFF}, V_{th} can not be largely scaled down. Therefore, the second term in eq.2 increases and consequently E_{eff} increases as the generation of bulk device advances.

In contrast, E_{eff} of i-body SOI-MOSFET is given by $E_{eff} = qN_s / 3\varepsilon_{Si}\varepsilon_0$. The equation does not have the second term which appears in the equation for bulk device [eqs.(1) or (2)]. Therefore, the difference in E_{eff} between the bulk and *i-body* devices is enhanced in small devices.

5.Comparizon in the switching speed Figure 7 shows the comparison on the switching speed of CMOS inverter, calculated by using a relation $\tau_{pd} = (C_{OX}+C_{SD}+C_{load})V_{DD} / I_{ON}$. A large I_{ON} of *i-body* device, which is originated from a small E_{eff}, greatly improves τ_{pd} of a small device. L-type 0.05 μm *i-body* double gate device shows nearly half τ_{pd} compared to that of bulk device.

6.Conclusions From a set of simulation, it was found that μ and I_{ON} enhancement in *i-body* SOI-MOSFET becomes remarkable as the device is miniaturized, since the E_{eff} of the device does not increase through the miniaturization. It was also shown that the advantages of *i-body* device are more remarkable in low stand-by power devices having large V_{th}.

Acknowledgment This work was partly supported by the New Energy and Industrial Technology Development Organization (NEDO).

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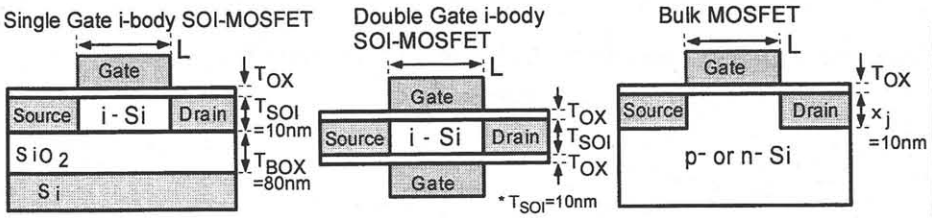

Fig. 1 Device structures

Table 1 ** $T_{OXeff} = T_{OX}+1nm$

MPU Gate Length L(μm)	0.25	0.18	0.10	0.08	0.05
V_{DD} (V)	2.5	1.8	1.2	1.0	0.8
T_{ox} (nm) **	6.0	3.8	1.9	1.5	1.0
H - type (nA/μm)	1	4	10	45	55
L - type (pA/μm)	1	4	10	45	55
Typical Wire Length [4] (μm)	460	374	257	223	165

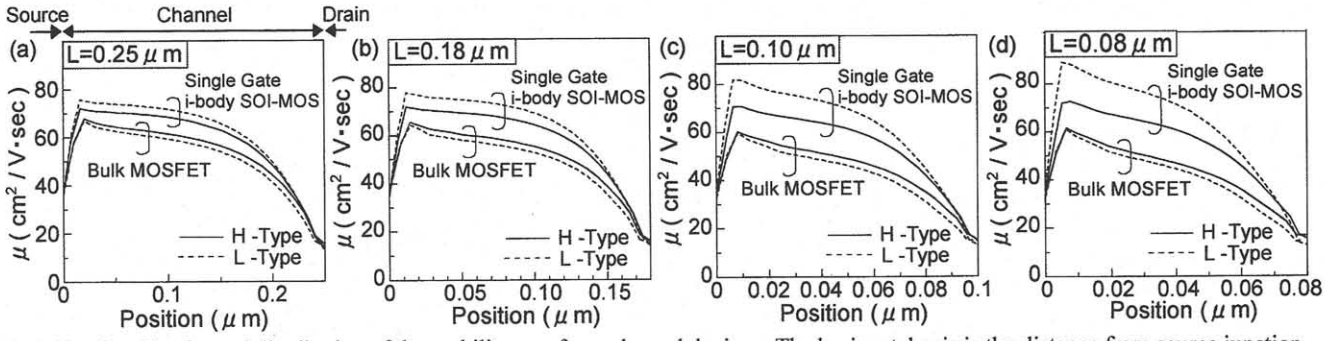

Fig.2 Simulated horizontal distribution of the mobility μ for p-channel devices. The horizontal axis is the distance from source junction.

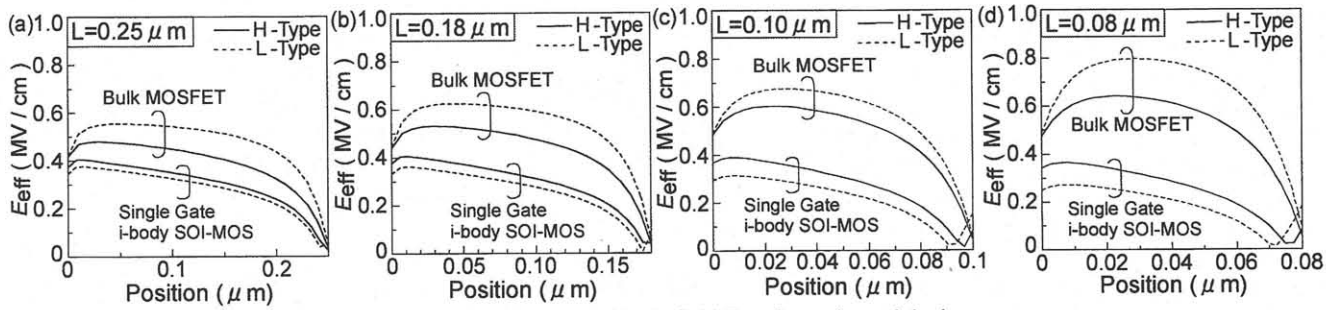

Fig.3 Simulated horizontal distribution of the effective normal electric field E_{eff} for p-channel devices.

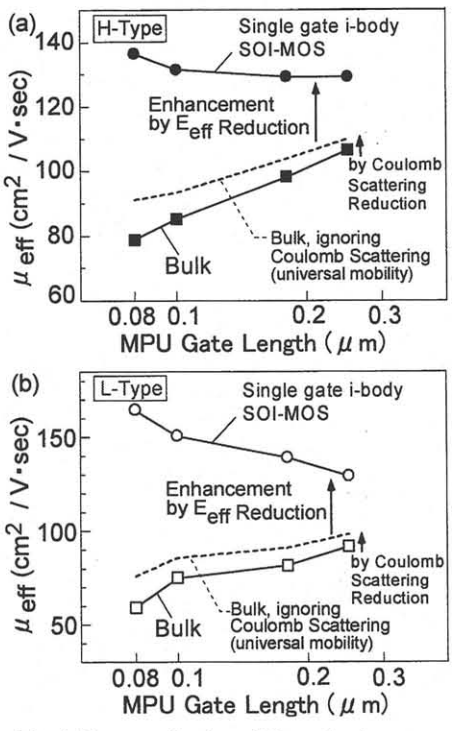

Fig.4 The contribution of E_{eff} reduction on μ_{eff} enhancement in p-channel devices. μ_{eff} is calculates at $L/5$ from the source junction.

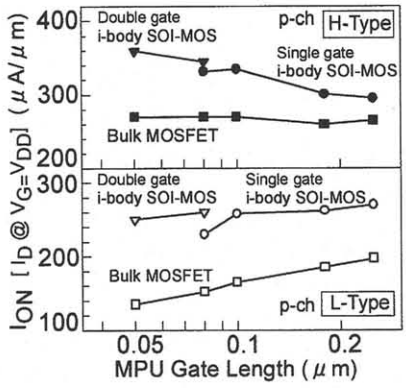

Fig.5 Calculated I_{ON} of p-ch devices.

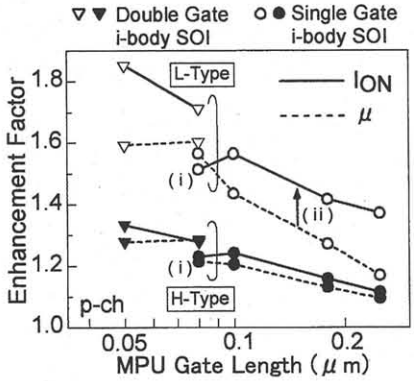

Fig.6 Enhancement factors on I_{ON} and μ.

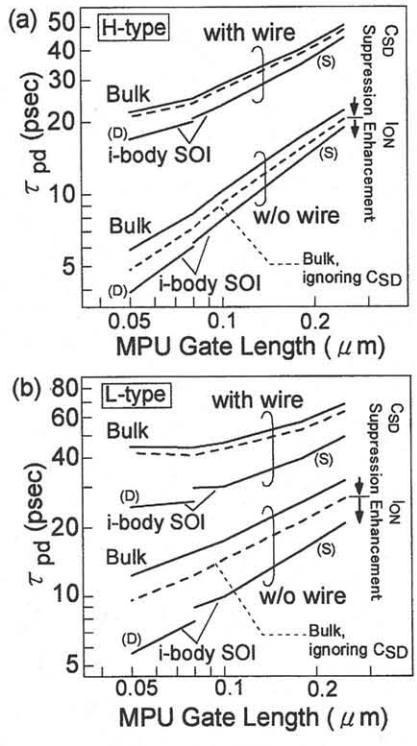

Fig.7 Calculated τ_{pd} of CMOS inverter, without wire and with wire of typical length [4]."(S)" is single gate, "(D)" is double gate.