Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 252–253

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A Simple Method to Fabricate Double-Gate SOI MOSFET with Diffusion Layer on Bulk Silicon Wafer as the Bottom Gate

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1. Introduction

There is a significant interest in the study of double gate SOI MOSFETs due to its immunity to short channel effects and its scalability to beyond the sub 0.1μm regime. However, the progress of double gate device related research is relatively slow due to the difficulty in device fabrication. Most of the studies on double gate structures have to be restricted to device simulation. In this paper, we have developed a simple method to fabricate double gate devices starting from bulk silicon wafer. The process relies on the crystallization of amorphous silicon film using nickel as the crystallization agent. But the process is generic enough to allow the use of other crystallization method such as selective epitaxial overgrow. The recrystallized silicon film (referred as LPSOI film [1]) has been carefully characterized and found to be equivalent to single crystal silicon film except with slightly higher defect density, similar to SOI wafers produced in the early days. As a result, all the physical properties of double gate SOI MOSFETs are preserved. The material quality and devices characteristics will also be reported.

2. Device Structure and Fabrication

The layout and schematic cross-section of the double gate SOI device is shown in Fig. 1. The bottom gate of the double gate device is formed by a diffusion layer on the bulk silicon which can be tied to the top gate of individually biased. The fabrication process is illustrated in Fig. 2. Starting with a bulk wafer, 250Å of oxide is grown followed by 1100Å of nitride deposition. The nitride and oxide stack is defined by the bottom gate mask. A semi-recessed LOCOS process is used to define the bottom gate dimension. Before the LOCOS, some silicon outside the nitride and oxide stack is removed to increase the abruptness of the bottom gate etch. Arsenic implantation is performed to dope the bottom gate after removing the nitride mask. The dose has to be carefully chosen not to create significant damage to the silicon structure. Thermal oxidation is performed to grown the bottom oxide. After that, 500-1000Å of amorphous silicon is deposited to become the body of the double gate MOSFET. Afterward, nickel induced crystallization similar to the one described in [1] is performed to crystallize the amorphous silicon layer to form a near single crystal silicon layer called LPSOI film. The temperature used for crystallization is 580°C for 24 hours, which is an improved condition to that reported in [1]. After recrystallization, 100Å of gate oxide is grown followed by polysilicon deposition and gate definition. The subsequent process follows that of a standard CMOS process. Unlike the gate-all-around process described in [2], the process is more simple and flexible expecially for wide devices. Fig. 3 shows the SEM cross-section of the fabricated device indicating the feasibility of the process.

3. Device Performance

Both single and double gate MOSFETs have been fabricated using the described method. Single gate SOI MOSFETs are also fabricated as a control wafer. The comparison of single gate SOI devices with single gate MOSFETs on the recrystallized film is shown in Fig. 4 indicating the recrystallized film is close to the high quality silicon film on SIMOX wafers. The difference in current comes from a slight the higher defect density of the recrystallized film compared with the high quality silicon film on SIMOX wafer.

The I-V characteristics of the double gate MOSFETs is shown in Fig. 5, together with a single gate device for comparison. The double gate device shows a higher current drive compared with the single gate devices. The increase in double gate device current is less than 2x of the single gate devices due to the slightly higher oxide thickness of the back gate. The subthreshold characteristics of the double gate MOSFET is shown in Fig. 6 indicating good immunity to short channel effects with a high subthreshold swing of 78mV/dec.

4. Conclusion

A simple process to fabricate double-gate device on from bulk wafer is presented. The device performance is similar to double-gate device fabricated on early day SOI films with higher defect density, which preserve all physical characteristics of a double gate SOI devices.

Acknowledgments:

This work is sponsored by a Competitive Earmarked Research Grant HKUST6190/01E from the Research Grant Council of Hong Kong. The authors would also like to thanks S. Leung of MCPF for his help in paper preparation.

Reference:

[1] H. Wang, et. al., *IEEE Transactions on Electron Devices*, vol. 47, no. 8, pp. 1580-1586, December 2000.
[2] V. W. C. Chan, et. al., Proceedings of 2000 International SOI Conferences, pp. 112.

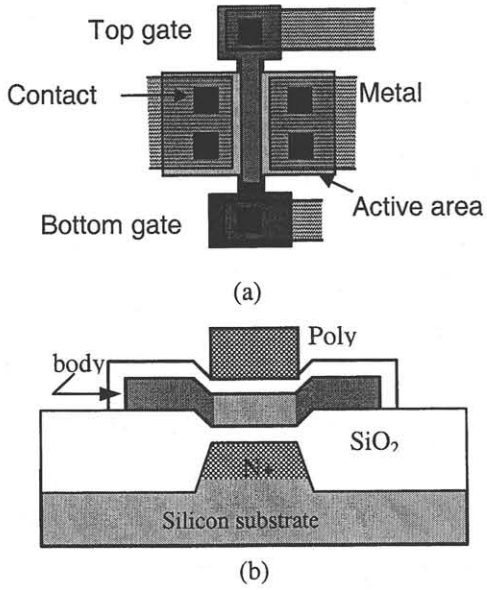

Fig.1. (a) Layout and (b) cross-section of the proposed double gate device structure.

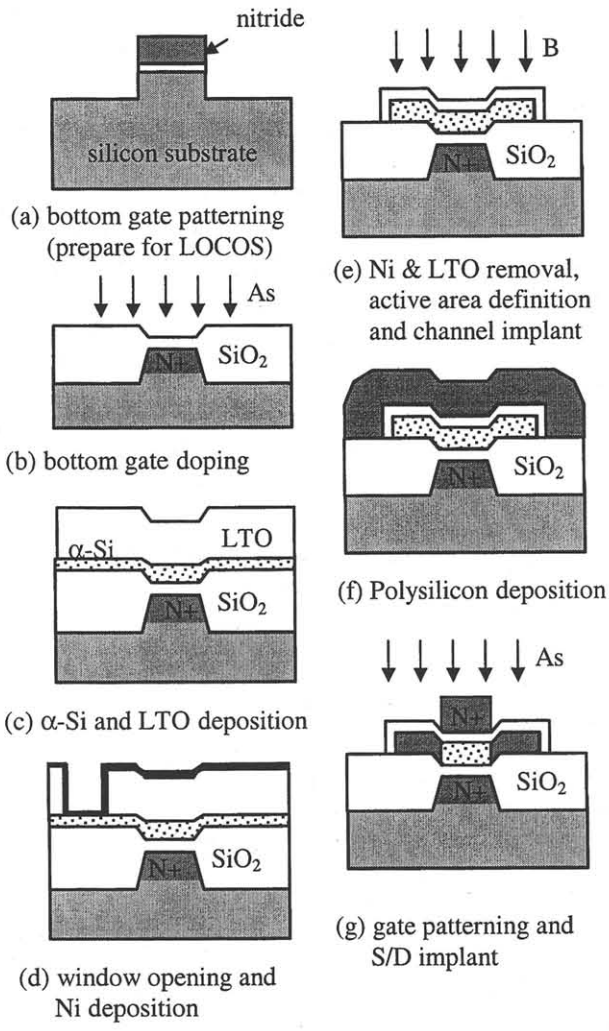

Fig.2. Fabrication process double gate devices

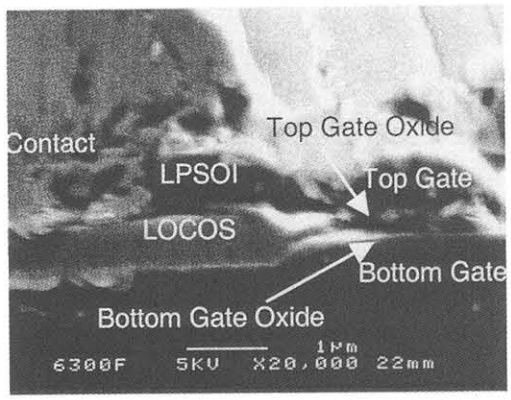

Fig.3. SEM picture of the proposed double gate device

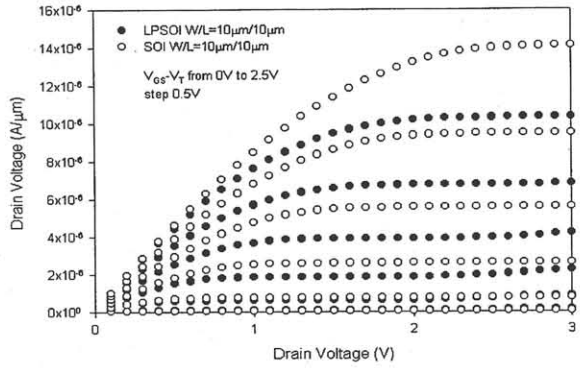

Fig.4. I-V characteristics of LPSOI and SOI MOSFET

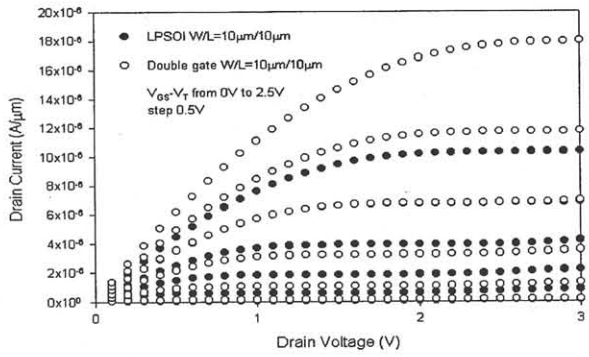

Fig.5. I-V characteristics of single and double gate LPSOI MOSFETs

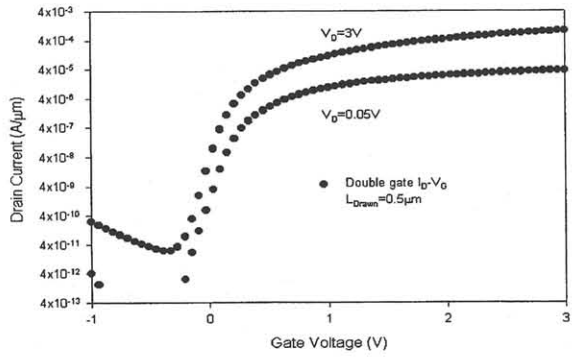

Fig.6. Subthreshold characteristics of a short channel double gate device