Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 256–257

C-5-1 (Invited)

SOI Technology for MPU Applicastions

Michael A. Mendicino

CMOS Platform Technology, Digital DNA Laboratories, Motorola
Austin, TX 78721, USA

1. Introduction

SOI technology is generally a good match with high performance products because improved speed and lower dynamic power are valued by the customer. These products are typically quite large and contain substantial onboard memory. Therefore, achieving high yield requires rigorous defect reduction efforts similar to bulk, and also robust solutions for SOI-specific material, process, and device interactions. Finally, to reap full advantage of the SOI opportunities, DC and transient floating-body effects (FBE) must be managed through careful device design and process integration. This work reviews some key aspects of a high performance SOI technology.

2. SOI Materials and High Performance Process

In the late 1990s, SOI wafer defect densities were reduced to levels comparable to bulk Si [1]. In that timeframe, however, material of various types and suppliers did tend to show corresponding variation in device parametrics, usually due to variation in film dopant concentration and/or recombination lifetime [2]. Today, further improvements in material quality and reduced sensitivity from the highly scaled devices, have nearly eliminated these issues.

An SOI process is different from bulk Si in the FEOL. It requires a new understanding of material, process, and device interactions, as well as SOI-specific defect metrology [3] and yield enhancement. Some interactions that may differ in SOI are: back interface effects and dopant redistribution, process induced damage response, local stress effects (mobility/defectivity), global stress effects, device scaling with floating-bodies, process and material controlled carrier lifetimes, defect and process metrology (reflectivity/charging), gettering, and effects of limited Si on integration. Figure 1 illustrates a case where local, isolation-related stress significantly impacts SRAM yield [4]. Here, the stresses induced in trench liner oxidation interacted unfavorably with subsequent oxidation and annealing in the gate module. A robust SOI solution, with thinner poly oxidation, was found to reduce sensitivity to the isolation process for a variety of SOI material types. There are numerous other cases such as this, where process modules or unit processes require modification to achieve high yield while preserving SOI advantages.

3. Device Technology

Performance optimization (DC):

SOI device performance optimization includes the traditional aspects from bulk, and those specific to SOI FBE. Figure 2 illustrates a progression of device optimization where efficient reduction of parasitic resistances shifted the Ion/Ioff universal curve, but also caused an increase in the off-state body voltage due to increased generation current. FB optimization was performed, which can involve extension and halo implant conditions and species, pre-amorhization implants, annealing, spacer process(es), and salicidation. These processes are tuned in such a way that the balance of generation and recombination currents occurs at a lower body voltage. Figure 3 illustrates this balance through forward and reverse bias (with impact ionization) diode measurements on body contacted devices [5]. As devices scale, other mechanisms affecting the balance such as gate leakage and gate induced drain leakage must be comprehended. At the same time, of course, parasitic capacitance must kept at a minimum for a given transistor node. Proper optimization of performance and DC body voltage is then reflected in product level performance at a given leakage as shown in Figure 4.

Managing Transient Floating Body Effects:

Another objective is minimization of the adverse transient FBE. Well-balanced devices that produce minimal history dependent delay variation can be obtained through careful optimization of generation and recombination currents, and capacitances [6]. Figure 5 illustrates how body voltage just before switching is determined by the various mechanisms of interest: , I) Gate-to-body (GTB) coupling, II) Drain-to-body coupling, III) recombination, and IV) GTB coupling. Devices should be centered in a regime that provides low history effects over a suitable range of operating voltages and temperatures, and also allows some Lpoly extendibility before full re-optimization is required.

In addition to proper device optimization, a high performance SOI technology should include a variety of devices to enable multiple ways to address floating body issues, so that an optimum solution can be implemented. This device lists may include, but is not limited to: multiple Vt and gate oxide thickness devices, low

parasitic body-contacted and source-body-tied devices, and well-designed diodes, capacitors and resistors.

4. Summary

SOI technology can offer significant advantage over bulk Si for high performance products. This requires a solid foundation of high quality SOI wafers, and a robust process, which accounts for interactions unique to the SOI wafer and device. Suppression of adverse AC and DC FBE is critical to realizing sufficient performance gain.

Acknowledgments

The author gratefully acknowledges the support for HiPerMOS SOI from the Dan Noble Center pilot line and Motorola Digital DNA Laboratories and the hard work of the SOI device, process, and integration teams.

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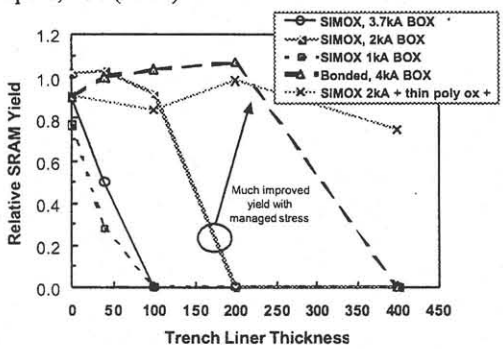

Figure 1 Yield versus trench liner thickness for various SOI material types, BOX thicknesses and process options. [4]

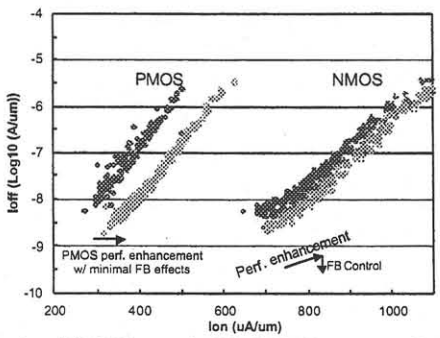

Figure 2 NMOS and PMOS Ion vs. Ioff as device performance improvements affect FB characteristics

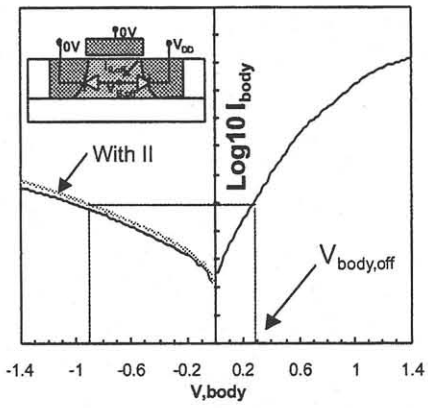

Figure 3 Vbody dependence on SOI diode characteristics with and without impact ionization.

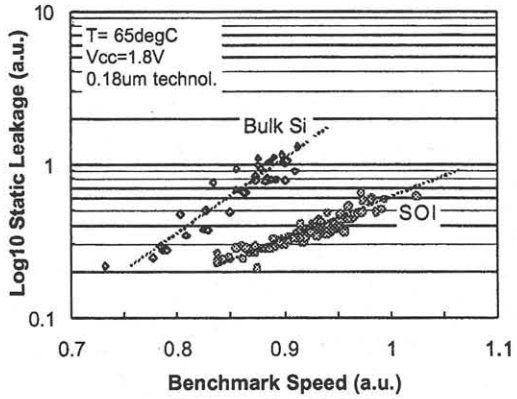

Figure 4 Normalized chip level benchmark performance versus static leakage for SOI and Bulk 0.18um technologies.

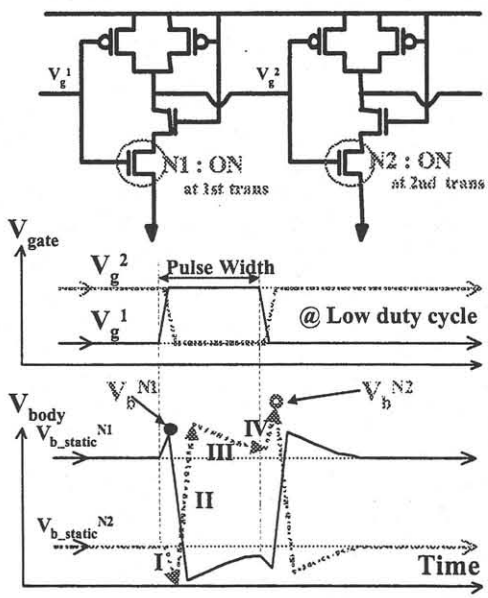

Figure 5 Schematic of a pair of stages in a 2-input nand chain, and the corresponding body voltage changes during a switching event.