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Low Voltage SOI Circuit Technology

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1. Introduction

The use of mobile equipment with communication functions has expanded rapidly in recent years. Considering the coming network computing era, the number and variety of mobile units is expected to increase much more. For such equipment, further miniaturization and longer battery-life are required. Ultralow-power design is essential for meeting these requirements. For CMOS LSIs, which are the key components of mobile equipment, lowering supply voltage and using SOI devices are the most effective design approaches for reducing power dissipation. We have proposed various 0.5-V multi-Vth SOI circuits and verified their effectiveness in some digital LSIs [1] [2]. To apply and expand our ultralow-voltage SOI circuit technology to LSIs in mobile equipment, we have to develop digital components, such as a CPU and a memory, and analog/RF components. A DC-DC converter that can convert the external apply voltage of the battery to the internal 0.5 V and has conversion efficiency of over 90 % is also required. In this paper, we overview a national ultralow-voltage SOI project called "R&D of Ultralow-power LSIs for Mobile Equipment" [3] and present some results for multi-Vth SOI circuits including analog/RF circuits and a DC-DC converter.

2. The SOI Project

The ultralow-voltage SOI project is one theme of the larger project, "Development of Immediately Effective and Innovative Technology for Energy and the Environment" [3], following the 1997 Kyoto conference (COP3) on the reduction of green house gases. Our project contributes to decrease the amount of carbon dioxide by reducing the power dissipation of the mobile equipment. Nine companies are involved in the project, which was started in 1998 and will continue until 2002. The organization of the project is shown in Fig. 1. There are three working groups. The device/process working group performs LSI fabrications with 0.25- and 0.35-μm SOI processes to verify the effectiveness of ultralow-voltage digital and mixed digital/analog circuits. An ultrathin-film fully-depleted SOI device, which is suitable for low-power and low-voltage operation, is adopted. This working group also deals with SOI device engineering, such as lowering the source/drain sheet resistance, the suppression of Vth-variation, and the scaling of SOI devices. The circuit simulation working group evaluates typical SOI device models, such as BsimSOI, BTASOI, and Florida. This group has also derived a universal parameter-extraction algorithm for these SOI device models. The circuit design working group consists of three sub-working groups related to a digital CMOS/SOI circuit, an analog/RF SOI circuit, and a DC-DC converter. All working groups corporate with one another through a project design manual based on LSI fabrications.

The relationship between application and LSI performance is shown in Fig. 2. SOI devices have already been used in ultrahigh-speed and micro-watt applications like server machines and watches, but they have not been applied to mobile equipment such as PDAs whose digital LSIs operate at 30~100 MHz. Their power dissipations are still over 100 mW. In the project, the power dissipation goal for the digital LSIs is 1~10 mW at 100-MHz operation. An example of target mobile equipment, which could be used for 2-GHz band wireless communication, is shown in Fig. 4. Applying the 0.5-V digital LSIs and the 0.5~1-V analog/RF LSIs, the project aims to make the power dissipation 1/10~1/100 that of conventional 3.3-V LSIs.

3. Some Results

A digital sub-working group has designed some digital components, including a 32-bit RISC processor based on pass-transistor logic, a multi-Vth SRAM, and ROM. The MTCMOS/SOI SRAM scheme [4] is shown in Fig. 4. Multi-Vth memory cell and readout-circuit scheme suppress the leakage current of the memory cell and make possible fast operation at 0.5 V. An analog/RF sub-working group is investigating 2-GHz and 300-MHz band RF circuits and a baseband analog circuit. Their 2-GHz band RF-mixer circuit [5] is shown in Fig. 5. The LC-tank current source and the folded circuit make possible 0.5-V operation by reducing a number of series-connected transistors in the differential circuit. A DC-DC converter sub-working group is concentrating on converters and ESD-immune I/O interface circuits. Two types of DC-DC converters, which convert external voltage of 1.2 V to internal voltage of 0.5 V, are shown in Fig. 7. One is switched-capacitor-type converter with serial-parallel switching, and the other is LC-filter-type converter [6]. High conversion efficiencies of over 85 % were obtained.

3. Conclusions

Severe ultralow-power requirement of 1-10 mW will be needed for future mobile-equipment use LSIs. To meet this requirement, we present some promising 0.5-V SOI technology with multi-Vth CMOS/SOI circuits. The national SOI project we overviewed will continue to develop and introduce more ultralow-voltage circuits.

Acknowledgment

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References

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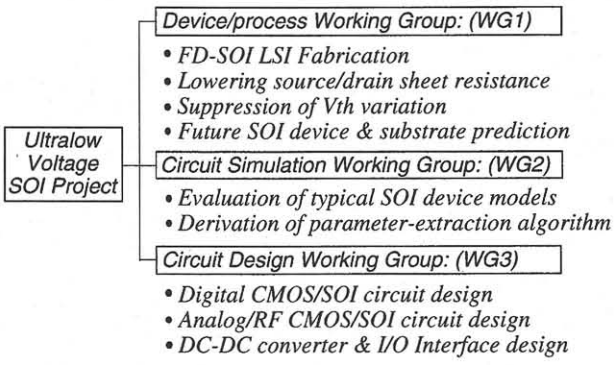

Fig. 1. Organization of the ultralow-voltage SOI project.

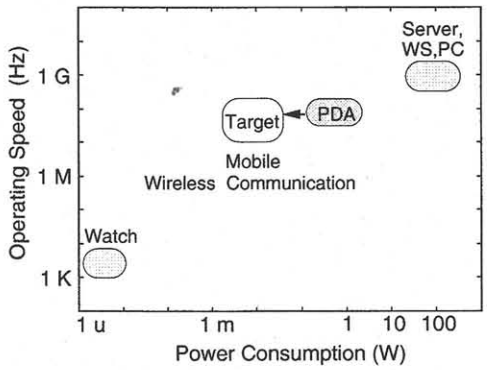

Fig. 2. Target application and LSI performance.

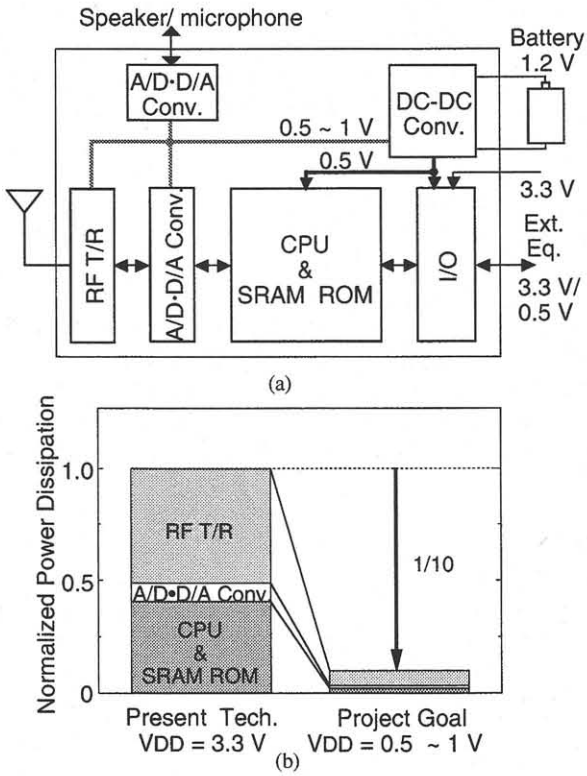

Fig. 3. Example of ultralow-power mobile equipment .
(a) Block diagram. (b) The power dissipation goal.

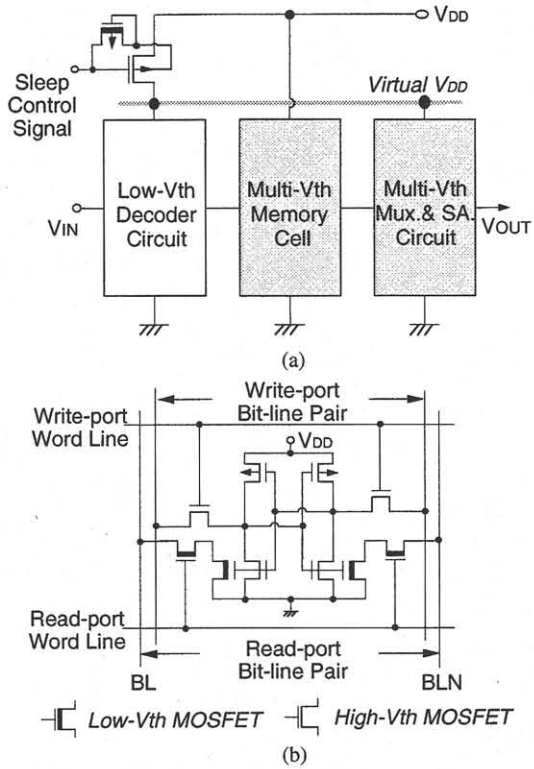

Fig. 4. The multi-Vth CMOS/SOI digital circuit scheme.
(a) The 0.5-V MTCMOS/SOI SRAM scheme.
(b) The multi-Vth memory cell .

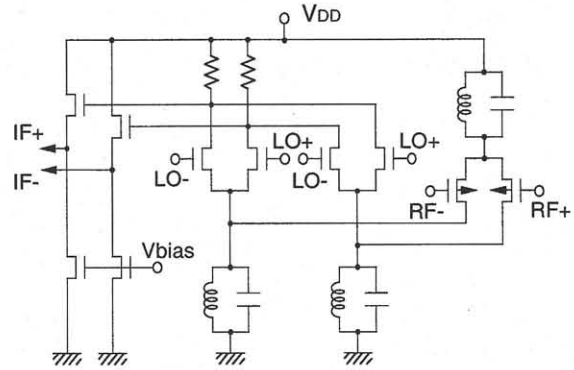

Fig. 5. The RF folded mixer with tank current source.

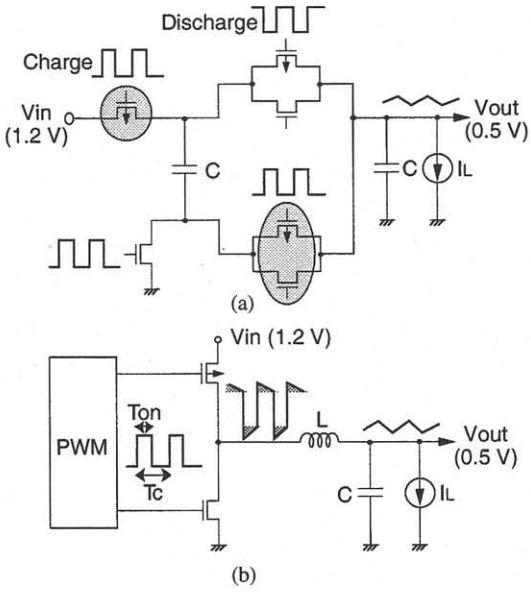

Fig. 6. 1.2/0.5-V DC-DC converter schemes.
(a) Switched-capacitor-type converter. (b) LC-filter-type converter.