

C-5-4

Effects of Gate-to-Body Tunneling Current on PD/SOI CMOS Circuits

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I. INTRODUCTION

Recently, the gate-to-body tunneling current in PD/SOI device resulting from the electron tunneling from the valence band (EVB) [1] has been shown to charge/discharge the floating-body, thus changing the body voltage and V_T and affecting circuit operations [2, 3]. In this paper, we present a detailed study on the effect of gate-to-body tunneling current on PD/SOI CMOS circuits in a 1.5 V, 0.18 μm PD/SOI technology with $L_{eff} = 0.075 \mu\text{m}$, $t_{ox} = 2.3 \text{ nm}$, $t_{Si} = 150 \text{ nm}$, and $t_{BOX} = 145 \text{ nm}$. Basic physical mechanisms underlying the variations in body voltage and delay and their temperature dependence in the presence of the gate-to-body tunneling current are examined. The resulting impacts on the gate delays and Power4 PowerPC microprocessor [4] critical paths are presented.

II. TEMPERATURE DEPENDENCE & INITIAL QUIESCENT STATE

Fig. 1 shows the temperature dependence of the "intrinsic" nMOS leakage, parasitic bipolar leakage, and gate-to-body tunneling current (I_{gb}) for a PD/SOI nMOS with $L_{eff} = 0.075 \mu\text{m}$. Two cases for the I_{gb} are shown, corresponding to two different biasing conditions for the nMOS; namely $V(G, S, D) = (0, 0, V_{DD})$, and $V(G, S, D) = (V_{DD}, 0, 0)$. As can be seen, the gate-to-body tunneling current exhibits a much weaker temperature dependence compared with the "intrinsic" nMOS leakage and parasitic bipolar leakage, hence its effects are expected to be more significant at lower temperature.

Consider a static CMOS inverter in the quiescent state with input initially at "Low" (Fig. 2(a)). For the nMOS, with $V(G, S, D) = (0, 0, V_{DD})$, its body sits at a diode cut-in voltage determined primarily by the balance of the back to back drain-to-body and body-to-source junctions. Thus, there is a "small" negative bias across the gate and body, resulting in "small" EVB from the gate to the body. This "small" body-to-gate tunneling current discharges the body, thus increasing V_T slightly and making the nMOS "slightly weaker". The body voltage of the nMOS is determined by the balance of the reverse-biased drain-to-body junction leakage current (which flows into the body), the body-to-gate tunneling current (which flows out of the body), and the forward-biased body-to-source junction current (which flows out of the body). For the pMOS, with $V(G, S, D) = (0, V_{DD}, V_{DD})$, its body sits at V_{DD} . Hence, there is a "large" negative bias across the gate and body, resulting in EVB from the gate to the body. This body-to-gate tunneling current discharges the body, thus decreasing V_T and making the pMOS "stronger". The body voltage of the pMOS is determined by the balance of the forward-biased drain-to-body and source-to-body currents (both flow into the body) and the body-to-gate tunneling current (which flows out of the body). When the inverter starts switching, because of the "slightly weaker" nMOS and "stronger" pMOS, the input-rise delay slows down while the input-fall delay speeds up (compared with the case when there is no gate-to-body tunneling current). The complementary situations hold for the case with the input initially at "High" (Fig. 2(b)). For this case, due to the "stronger" nMOS and "slightly weaker" pMOS, the input-rise delay speeds up while the input-fall delay slows down.

III. STATIC CMOS INVERTER

Fig. 3(a) shows the input-rise delays as functions of time with temperature as a parameter for a PD/SOI CMOS inverter "without" the gate-to-body tunneling current. The inverter input is initially at "Low" and then switches continuously at 1.0 GHz with 50% duty cycle and 100 ps input slew. The load, 50 fF, is equivalent to a fan-out of 3 for the device sizes used. The body voltages for the nMOS are shown in Fig. 3(b). The corresponding cases, with the gate-to-body tunneling current, are shown in Fig. 4(a) and 4(b), respectively. As the initial nMOS body voltage is determined primarily by the balance of the back to back

drain-to-body and body-to-source diodes, both the initial nMOS body voltage (Fig. 3(a)) and the initial input-rise delay (Fig. 3(b)) exhibit strong temperature dependence [5]. Furthermore, as can be seen in Fig. 4(b), the body is only slightly discharged by the body-to-gate tunneling current.

Fig. 5(a) and 5(b) show the complementary situation, where the inverter input is initially at "High", "without" the gate-to-body tunneling current. The corresponding cases, with the gate-to-body tunneling current, are shown in Fig. 6(a) and 6(b), respectively. With the input initially at "High", the body voltage of the nMOS before the first input-rising transition is determined primarily by capacitive coupling and exhibits weak temperature dependence (evident by the "clustering" of the initial body voltages in Fig. 5(b), and the weak temperature dependence of the initial input-rise delay in Fig. 5(a)) [5]. Furthermore, as there is full V_{DD} across the gate and the body, the charging of the body by the gate-to-body tunneling current is quite significant (Fig. 6(b)). The effect can also be seen to be more significant at lower temperature, causing "spread" of the initial body voltages (hence initial input-rise delay as well).

IV. IMPACT ON CIRCUIT DELAYS

Fig. 7(a) and 7(b) show the percent changes in the inverter input-rise delay due to the gate-to-body tunneling current for the two initial conditions with $C_{load} = 17 \text{ fF}$ (equivalent to fan-out of 1). The percentage change in the delay is defined as $[(\text{Delay without } I_{gb}) - (\text{Delay with } I_{gb})] / (\text{Delay without } I_{gb}) \times 100\%$. As expected, with the input initially at "Low", the input-rise delay slows down with I_{gb} and the effect is more pronounced at lower temperature (Fig. 7(a)). At 25 °C, the slow-down is 9.5% initially and 4.4% at $t = 5000 \text{ ns}$. For the case of initially "High" input, the input-rise delay speeds up. At 25 °C, the speed-up is 1.75% initially and 0.0% at $t = 5000 \text{ ns}$.

Fig. 8(a) and 8(b) show the corresponding cases for the input-fall delay (dictated by the pMOS). The effect of I_{gb} can be seen to be more significant. For example, with input initially at "low" at 25 °C, the input-fall delay speed-up is 15% initially and 8.0% at $t = 5000 \text{ ns}$.

Fig. 9 shows the path counts vs the percent changes of the path delays due to I_{gb} at 85 °C for critical paths in the 1.0 GHz 170 million transistors Power4 PowerPC microprocessor [4]. The presence of I_{gb} can be seen to affect the path delays ranging from 4.0% slow-down to 6.0% speed-up.

V. CONCLUSION

In summary, the presence of gate-to-body tunneling current changes the strength of individual transistor in the quiescent state, thus affecting circuit delays when the circuit subsequently switches. The effect is more pronounced at lowered temperature. The impact on the gate delays and microprocessor critical path delays are significant with $t_{ox} = 2.3 \text{ nm}$ in a 1.5 V, 0.18 μm , $L_{eff} = 0.075 \mu\text{m}$ PD/SOI technology. With thinner gate oxide in scaled devices, a full understanding of the effect is crucial to ensure proper circuit functionality and performance.

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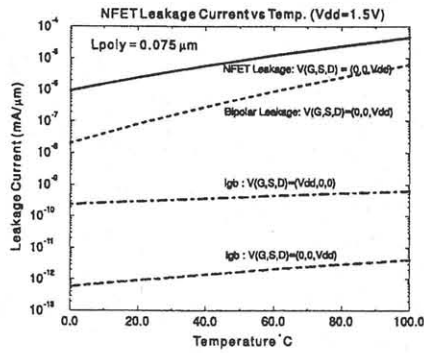


Fig. 1: Temperature dependence of "intrinsic" nMOS leakage, parasitic bipolar leakage, and gate-to-body tunneling current (I_{gb}) in a PD/SOI nMOS.

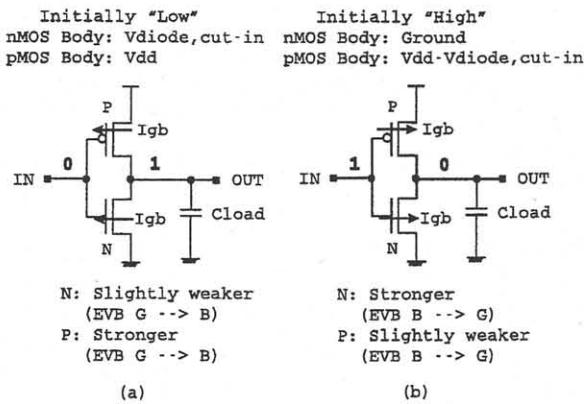


Fig. 2: A PD/SOI CMOS inverter in quiescent state with input (a) initially at "Low", and (b) initially at "High".

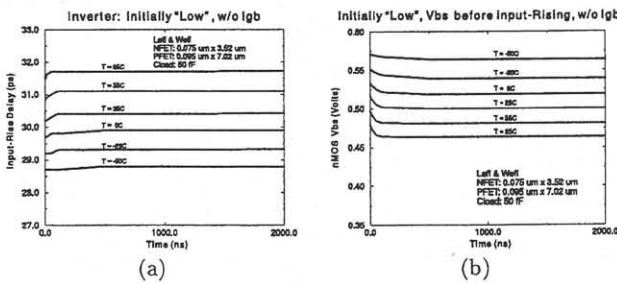


Fig. 3: (a) Input-rise delays, and (b) nMOS body voltages before the "input-rising" transitions as functions of time for a PD/SOI CMOS inverter (initially "Low") without I_{gb} (Cload = 50 fF).

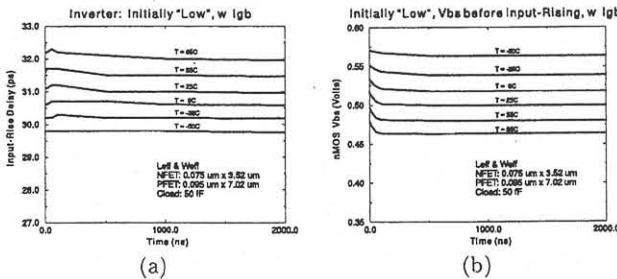


Fig. 4: (a) Input-rise delays, and (b) nMOS body voltages before the "input-rising" transitions as functions of time for a PD/SOI CMOS inverter (initially "Low") with I_{gb} (Cload = 50 fF).

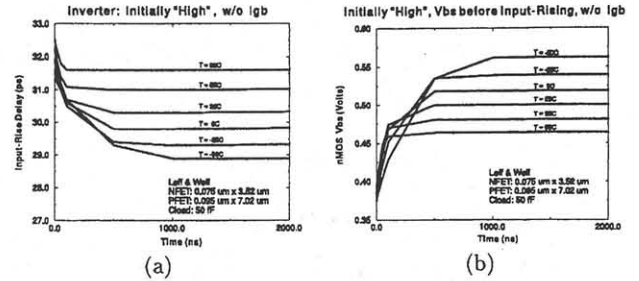


Fig. 5: (a) Input-rise delays, and (b) nMOS body voltages before the "input-rising" transitions as functions of time for a PD/SOI CMOS inverter (initially "High") without I_{gb} (Cload = 50 fF).

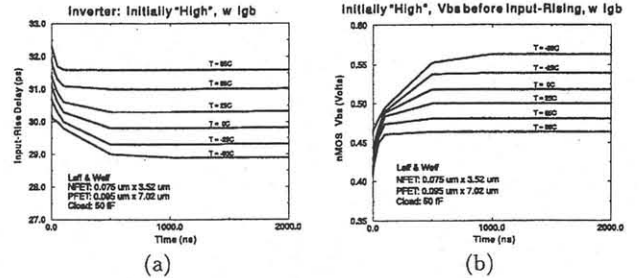


Fig. 6: (a) Input-rise delays, and (b) nMOS body voltages before the "input-rising" transitions as functions of time for a PD/SOI CMOS inverter (initially "High") with I_{gb} (Cload = 50 fF).

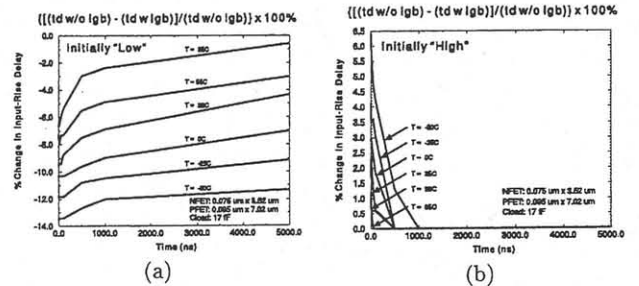


Fig. 7: Percent changes in inverter input-rise delays (Cload = 17 fF) due to I_{gb} for (a) initially "Low", and (b) initially "High".

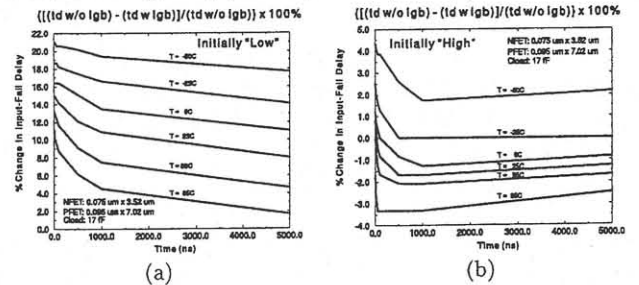


Fig. 8: Percent changes in inverter input-fall delays (Cload = 17 fF) due to I_{gb} for (a) initially "Low", and (b) initially "High".

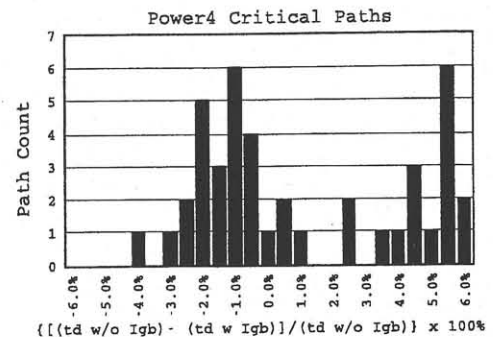


Fig. 9: Path counts vs percent changes of path delays due to I_{gb} at 85°C for critical paths in Power4 microprocessor