

C-5-5**A 0.5-V, Over 1-GHz, 1-mW MUX/DEMUX Core with Multi-Threshold Zero-V_{th} CMOS/SIMOX Technology**Takakuni Douseki, Fumiharu Morisawa, Shunji Nakata, and Yusuke Ohtomo¹

NTT Telecommunications Energy Laboratories,
 3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-0198 Japan
¹NTT Electronics Corporation, Ebina-shi, Kanagawa, Japan

1. Introduction

Sub 1-V CMOS circuit technology on ultrathin-film SOI devices is the most effective candidate for ultralow-power applications in future ULSIs. We have proposed various fully-depleted multi-threshold CMOS/SIMOX circuits [1] [2] that operate at an ultralow supply voltage of less than 0.5 V. In applying this technology to ultrahigh-speed LSIs with operating speed over 1 GHz, such as frequency dividers, the design of the threshold voltage of the low-V_{th} CMOS circuit is most important. For ultrahigh-speed LSIs, it is possible to set the threshold voltage of low-V_{th} CMOS circuit lower than that for the digital logic LSIs. This is because the ultrahigh-speed LSIs have a high activity ratio of operating gates, which makes it possible to enlarge the ratio of the dynamic and static power dissipation. But, making the threshold voltage too low causes the increase of the short-circuit power dissipation in addition to the static power dissipation due to the leakage current. The maximum operating frequency of the reported 0.5-V LSIs with threshold voltage of 0.2 V is less than 400 MHz [3]. In this paper, we describe zero-V_{th} CMOS/SIMOX circuit technology without any increase of the short-circuit power dissipation and verify its effectiveness in ultrahigh-speed multiplexer and demultiplexer (MUX/DEMUX) circuits.

2. Zero-V_{th} CMOS/SIMOX Design

The multi-V_{th} DEMUX and MUX circuit scheme is shown in Fig. 1. The ultrahigh-speed circuit block is a clock generator for both MUX/DEMUX circuits. So, a TFF and its CMOS clock driver, which consists of the clock generator, must use lower-V_{th} MOSFETs. The dependence of the delay time of the CMOS inverter on the threshold voltage is shown in Fig. 2. The characteristics of bulk devices whose junction capacitance is 10 times larger than that of FD-SIMOX devices are also shown for comparison. In addition to the SIMOX devices' providing high-speed operation, they keep the slew rate, the output rise time or fall time, almost all constant for positive threshold voltage. This is because the capacitance between the input and output of the CMOS inverter makes the output rise above the supply voltage due to a feed-forward effect (Fig. 3). Even though the feed-forward effect causes the increase of the delay time [4], the steep slew rate makes possible the suppression of the short-circuit power dissipation. The short-circuit power dissipation of the zero-V_{th} CMOS/SIMOX circuit is less than 10 % that of the dynamic power dissipation. On the other hand, the short-circuit power dissipation of the zero-V_{th} CMOS/bulk circuit is about half that of the dynamic power dissipation. The dependence of the maximum operating frequency on the

threshold voltage of a TFF is shown in Fig. 5. The dual-rail TFF [5] was used for high-speed operation. The maximum operating frequency is 1.7 GHz at zero-V_{th} CMOS/SIMOX circuit. The higher threshold-voltage for multi-V_{th} CMOS/SIMOX circuits is set to 0.15 V so that the operating frequency is more than half that of zero-V_{th} circuit. The dependence of operating frequency and power dissipation of the DEMUX and MUX on the lower threshold-voltage is shown in Fig. 6. For the DEMUX circuit with zero-V_{th} CMOS/SIMOX technology, the maximum operating frequency is 1.65 GHz and the power dissipation is 1.2 mW. For the MUX circuit, the maximum operating frequency is 1.4 GHz and the power dissipation is 1.34 mW.

3. Experimental Results

To verify the effectiveness of the zero-V_{th} circuit design, we designed and fabricated a MUX and DEMUX with 0.25- μ m MTCMOS/SIMOX technology [2]. The thicknesses of the gate-oxide, the active silicon layer, and the buried-oxide in the SIMOX-wafer are 5, 50, and 100 nm, respectively. The values of the threshold voltage of the zero-V_{th} and high-V_{th} MOSFETs are -0.02 and 0.17 V for nMOSFETs and 0.01 and -0.17 V for pMOSFETs. The operating waveforms of the DEMUX and MUX are shown in Fig. 7. The supply voltage is 0.5 V. The input patterns of the DEMUX and the MUX are "1001100011100000" and "01011010", respectively. The maximum operating frequency of the DEMUX is 1.7 GHz and the power dissipation is 1.3 mW. The maximum operating frequency of the MUX is 1.4 GHz and the power dissipation is 1.4 mW. Both circuit performances are summarized in Fig. 8. Both circuits make possible ultrahigh-speed operation over 1 GHz per 1-mW power dissipation.

4. Conclusions

Zero-V_{th} CMOS/SIMOX circuit technology with small short-circuit power dissipation was described. Using this technology, we demonstrated a 0.5-V multiplexer and demultiplexer that operate at more than 1 GHz with 1-mW ultralow-power dissipation.

Acknowledgments

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References

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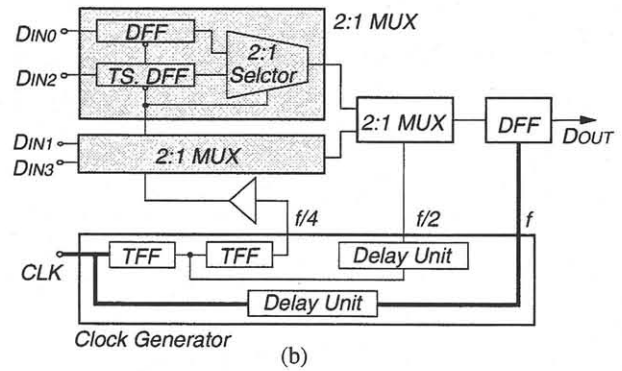
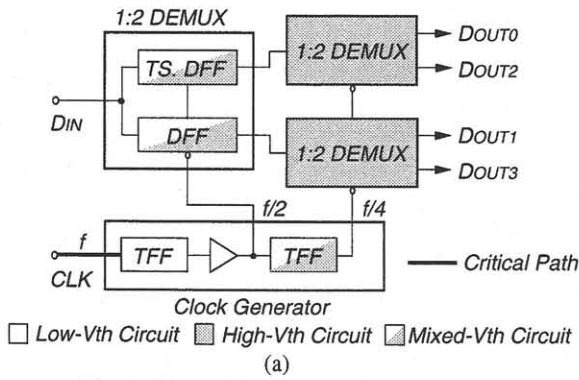


Fig. 1. The multi-Vth demultiplexer and multiplexer (DEMUX/MUX) scheme. (a) 1:4 DEMUX, (b) 4:1 MUX.

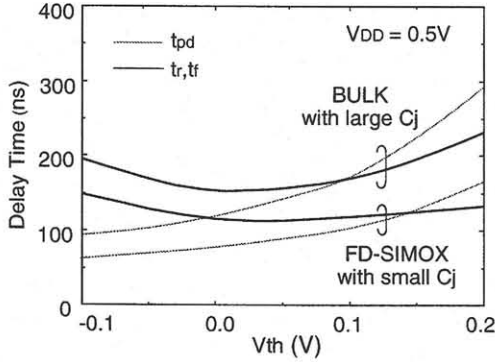


Fig. 2. Dependence of the delay time on the threshold voltage of the CMOS inverter.

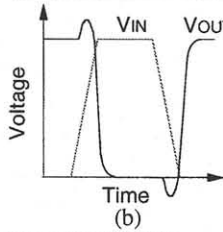
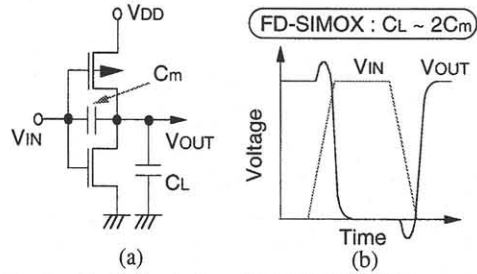


Fig. 3. The fully-depleted CMOS/SIMOX inverter with F/O = 1 and its response. (a) Equivalent circuit, (b) Feed-forward effect.

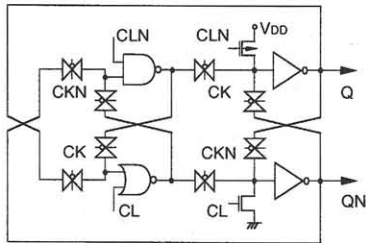


Fig. 4. The dual-rail TFF circuit.

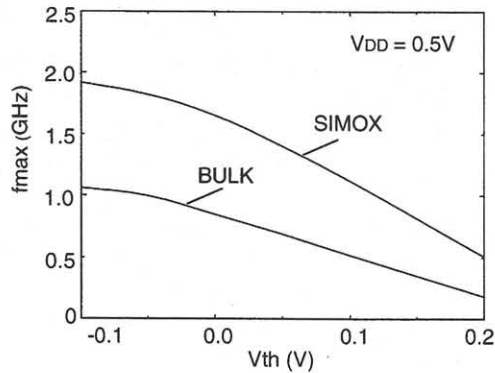


Fig. 5. Dependence of the maximum operating frequency on the threshold voltage of the dual-rail TFF circuit.

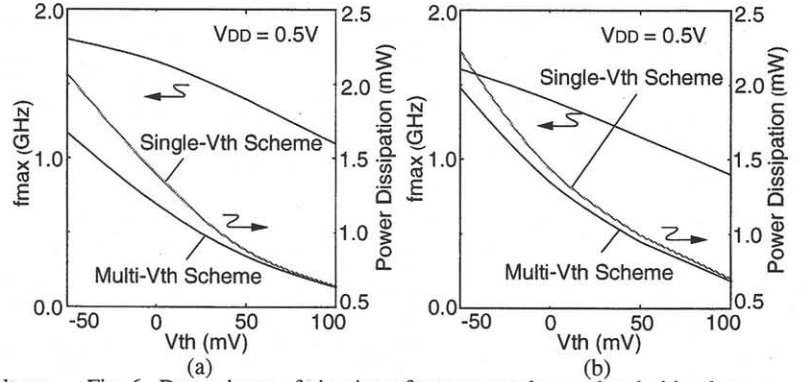


Fig. 6. Dependence of circuit performance on lower-threshold voltage. (a) DEMUX, (b) MUX

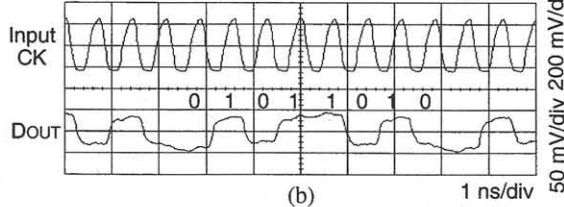
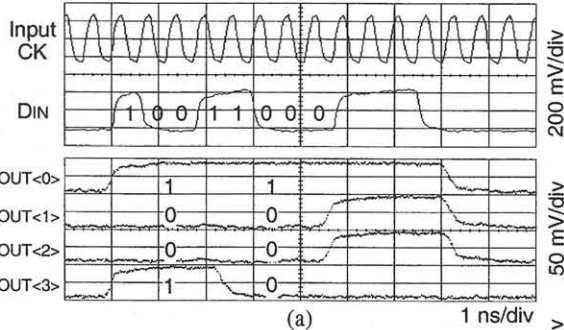


Fig. 7. Input and output waveforms of the DEMUX/MUX circuits. (a) Waveforms of DEMUX ($f = 1.7$ GHz), (b) Waveforms of MUX ($f = 1.4$ GHz).

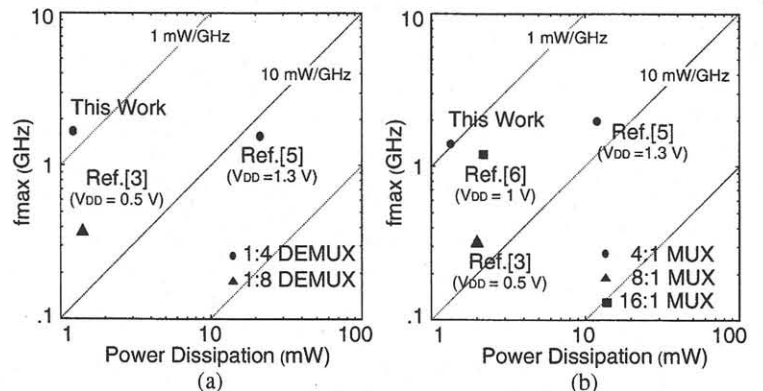


Fig. 8. Comparison of the present circuits with the conventional circuits. (a) DEMUX, (b) MUX.

