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Scenario of Source/Drain Extension and Halo Engineering for High Performance 50 nm SOI-pMOSFET

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1. Introduction

Due to recent aggressive scaling, minimum gate length (L_g) of MOSFET reached at sub 50 nm [1,2]. Shallower and steeper source/drain extension (SDE) with lower sheet resistance is required for scaling high performance CMOS. However, in pMOSFET the abruptness of SDE is not improved dramatically even by state-of–art spike annealing (SA) [3]. Without improvement of junction abruptness, degradation of drive current is expected due to large external resistance and small coupling between SDE and gate at 0.1 μm generation (50 nm physical gate length) pMOSFET [4,5]. Therefore SDE and halo engineering is very important to compromise drive current degradation and high performance in 50 nm pMOSFET. When reduction of gate capacitance is larger than current degradation, CV/I can be improved by decreasing L_g (fig. 1). In this paper we describe scenario of SDE and halo engineering for high performance 50 nm SOI pMOSFET which minimizes CV/I.

2. Experiment

Deep sub micron pMOSFET was fabricated on SOI substrate. The SOI thickness was 150 nm. A SiON gate dielectric film with T_{ox}^{inv} = 2.5 nm was used. A poly-Si gate was fabricated by e-beam lithography and dry etching. SDE dose, halo dose and SA temperature were optimized to realize high performance 50 nm SOI pMOSFET with minimum CV/I.

Electrical characteristics of SOI pMOSFET were taken by dc measurement under body contact conditions. Therefore, floating body effect is eliminated but self-heating effect is included in the electrical data.

3. Results and Discussion

Fig. 2 and 3 show SDE dose dependence of drive current, minimum gate length (L_{min}) and CV/I at I_{off} = 10 nA/μm. Halo dose was adjusted to obtain same V_{th} at L_g = 0.2 μm in each device. The SDE conditions used in this experiment have almost same abruptness as shown fig. 4. By decreasing SDE dose the short channel effect (SCE) is suppressed due to reduction of the junction depth and the overlap between SDE and gate. Drastic drive current degradation is observed at lowest SDE dose as reported in Ref. [4,5]. However, due to the reduction of L_{min}, CV/I is improved by decreasing SDE dose, even at the lowest dose where drive current degradation is observed (fig. 3).

Fig. 5 and 6 show halo dose dependence of drive current, L_{min} and CV/I at I_{off} = 10nA/μm. Although SCE is suppressed by increasing halo dose, drive current is also decreased monotonically (fig. 5). The CV/I value has minimum at an optimum halo dose (fig. 6). For smaller halo dose the drive current degradation is compensated by reduction of gate capacitance due to shorter L_{min} and the CV/I value continues to decrease with L_{min}. But for larger halo dose the drive current degradation is so severe that the CV/I value is increased.

At lower SA temperature the drive current is smaller in any SDE and halo conditions. But due to smaller L_{min} lower SA temperature gives smaller CV/I.

To realize a 50 nm SOI pMOSFET with minimum CV/I value the lowest dose SDE and an optimum dose halo were used since drive current degradation was smaller when L_{min} was decreased by reduction of SDE dose (fig. 7). A 50 nm SOI pMOSFET operates properly by the lowest dose SDE, an optimum dose halo and lower SA temperature (fig. 8 and 9). The drive current of the 50 nm pMOSFET is 292 μA/μm at I_{off} = 10 nA/μm. The drive current improvement is 3% when self-heating effect is removed by pulse measurement.

The CV/I improvement has been achieved in the 50 nm SOI pMOSFET. Its CV/I value is 2.85 psec at I_{off} = 10nA/μm, which is smaller than those of SOI pMOSFETs with higher drive current and longer gate length (fig. 10).

4. Conclusion

The SDE and halo optimization has realized the CV/I improvement up to 50 nm SOI pMOSFET even under drive current degradation condition. The minimum CV/I of 2.85 pesc is obtained in a 50 nm SOI pMOSFET with low dose SDE, an optimum dose halo and low thermal budget.

References

[1] R. Chau et. al., IEDM Tech. Digest p.45, 2000.
[2] H. Wakabayashi et. al., IEDM Tech. Digest p.49, 2000.
[3] A. Ono et. al., Symp. VLSI Tech. Digest p. 14, 2000.
[4] S. Thompson et. al., Symp. VLSI Tech. Digest p.132, 1998.
[5] T. Ghani et. al., Symp. VLSI Tech. Digest p. 174, 2000.

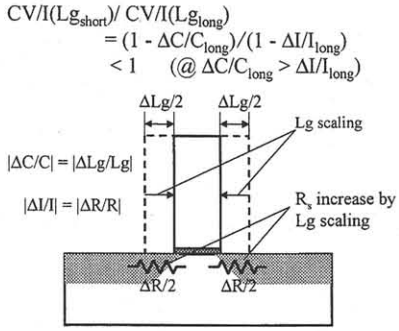

Fig. 1 CV/I improvement scenario by L_g scaling under drive current degradation condition.

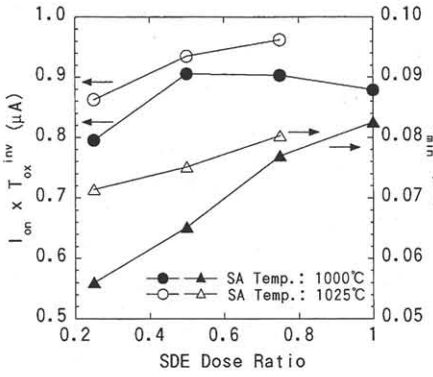

Fig. 2 SDE dose dependence of drive current and L_{min}.

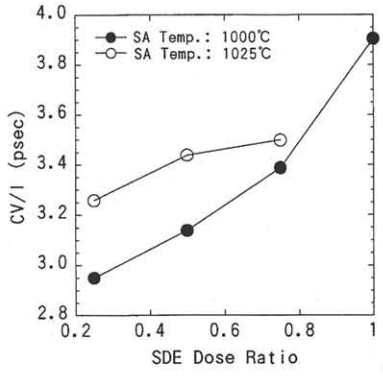

Fig. 3 SDE dose dependence of CV/I.

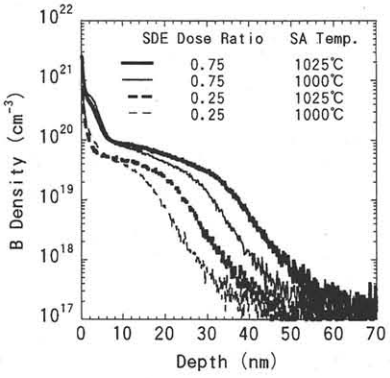

Fig. 4 Typical SIMS profile of SDE used in this experiment.

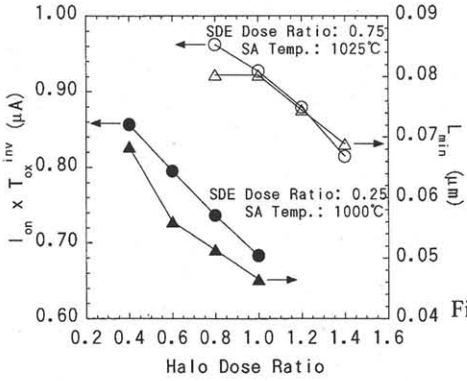

Fig. 5 Halo dose dependence of drive current and L_{min}.

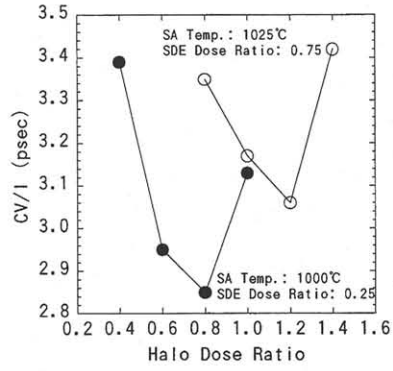

Fig. 6 Halo dose dependence of CV/I.

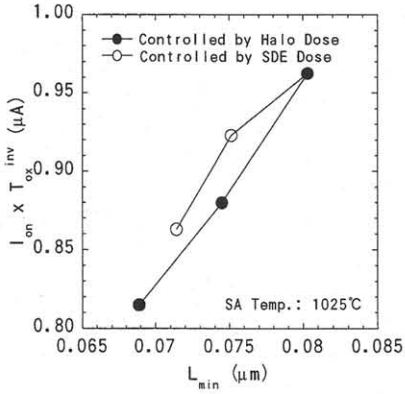

Fig. 7 Relationship between L_{min} and drive current controlled by SDE dose and halo dose.

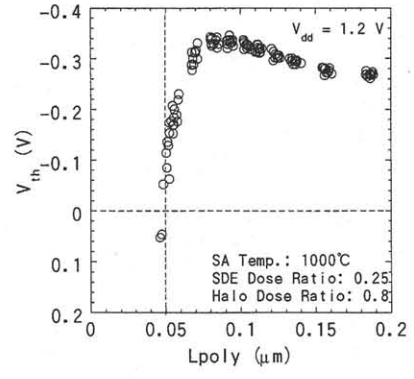

Fig. 8 Roll-off characteristics of pMOSFET with the lowest dose SDE, an optimum dose halo and lower SA temperature.

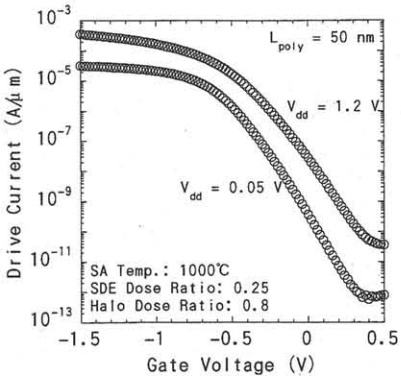

Fig. 9 V_g-I_d characteristics of 50 nm pMOSFET.

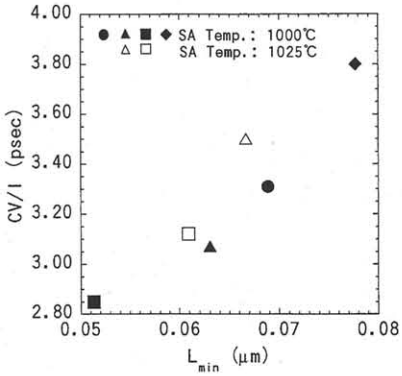

Fig. 10 Relationship between L_{min} and minimum CV/I.