Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 276–277

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Anomalous Noise Degradation Caused by Device Size Effects in SOI MOSFETs

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1. INTRODUCTION

Recently, it has been reported that the degradation /enhancement of mobility for the LOCOS isolated SOI MOSFET is due to the silicon strain resulting from volumetric expansion of the field oxide during thermal oxidation [1]. Also the mobility degradation for STI and MESA isolated SOI devices is attributed to the increased scattering in the SOI film [2]-[4]. For STI in bulk-Si, the abrupt transient region between STI and channel has a significant influence on the electrical characteristics of MOSFETs [5], [6]. In this paper, we report the influence of STI edge effects using the charge pumping method and low frequency noise characteristics.

2. DEVICE AND TEST STRUCTURES

Devices are fabricated using the sub-0.2 μm dual poly (n+/p+) gate PD-SOI on p-type 8" SIMOX wafers with Si film thickness of 100 nm and BOX of 100 nm. Gate oxide thickness is 3.8 nm. Fig. 1 shows three different types of test structure. First, the channel region of H-gate structure is not butted to STI region, which means that STI process does not affect H-gate. Second, in T-gate devices, one of the edges of the channel with is butted to the STI and the other is butted to the active channel region. Both sides of the channel region of I-gate structure devices are butted to STI.

3. ELECTRICAL CHARACTERISTICS

We have investigated in Ref. [7] that the degradation of MOSFETs in electrical characteristics of SOI MOSFETs with STI structure is found to be dependent on the device size. The degradation is due to transconductance and mobility decrease in N/P MOSFETs caused by the interface roughness (or damage) between STI and channel formed during the dry etch process and becomes significant with the decrease of channel width and the increase of channel length. In addition, the yield of the N/P MOSFETs is highly dependent on the width of the device. The comparison of the yields with three gate structures. Among SOI devices, the failure rate of the I-gate devices is very high while the H-gate devices, which are not affected by STI, show very low failure rate [7]. We can observe that the failure rate increases as the channel length increases at fixed width, and is more severe than inverse narrow width effects [7]. It is due to the process damage occurred at the side-wall of Si film during plasma etch of the Si film and the buried oxide The schematic illustration of fixed base level charge pumping (CP) measurement is shown in inset of Fig. 2. The measured I_{CP} for the T-, H-gate structures with various widths are shown in Fig. 2. According to the CP theory, CP current should be proportional to the device width at fixed length. In order to compare directly, we normalized the measured current to 0.25 μm of width. In Fig. 2 (a), an anomalous normalized I_{CP} (I_{CPN} = 0.25*I_{CP}/W) is measured in which I_{CP} increases with decreasing width (from 20 μm to 0.25 μm) in T-gate. It is due to the increased influence of ΔN_{it} located at the STI/channel interface for narrow-width devices. For a set of

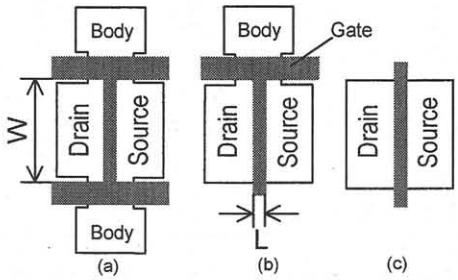

Fig.1. Top view and cross sectional view with (a) H-gate, (b) T-gate, and (c) I-gate.

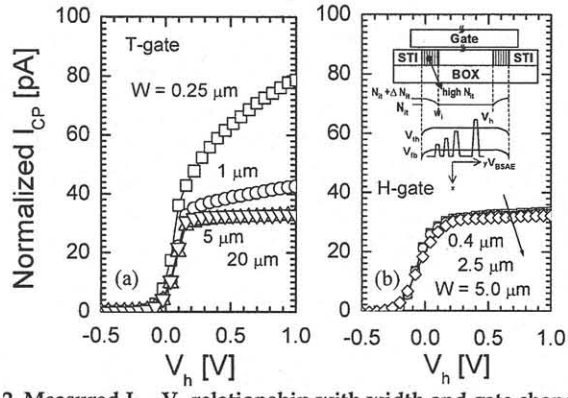

Fig. 2. Measured I_{CP}–V_h relationship with width and gate shape. (a) normalized I_{CP} of T-gate structure, (b) normalized I_{CP} of H-gate, respectively (Measurement conditions: f =100 kHz, Duty cycle = 50%, V_{BSAE} = -0.5 V, V_{step} = 0.06 V, V_h = 1 V, and Slope = 1 V/μsec). Cross sectional view of MOSFET and schematics of the fixed level charge pumping method are shown in the inset of (b).

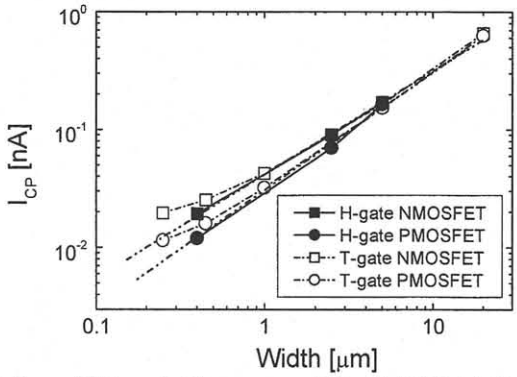

Fig. 3. I_{CPmax} (@V_h = 1 V) versus width of NMOSFETs and P MOSFETs with H- and T-gate (I_{CPmax} = qfN_{it}LW).

MOSFET without STI edge effect (Fig.2 (b)), its I_{CPN} is constant for various widths (Fig. 2) because H-gate structure is not butted to the STI. In Fig. 3, we can observe that the decrease rate of the I_{CP} of T-gate device slows down at the width of 1 μm, but the I_{CPmax} of the H-gate decreases in proportion to the device width because of the above reason. From Figs. 2 and 3, we consider the incremental charge pumping current as the difference between I_{CPN} of narrow

width devices and I_{CPN} of wide width devices at the fixed channel length and given by

$$\Delta I_{CP} = I_{CPN}(narrow) - I_{CPN}(wide) \approx fqL \int_0^{W_i} \Delta N_{it}(y)dy \frac{1}{W_{narrow}} \quad (1)$$

where ΔI_{CP}, I_{CPN}, f, q, L, ΔN_{it}, and w_{narrow} are the incremental charge pumping current, normalized charge pumping current, measurement frequency, charge, channel length, influence of interface–state density in w_i (high N_{it} region in inset of Fig. 2(b)), and the width of narrow device, respectively.

Low frequency noise characteristics with H-, T-, I-gate structure is shown Fig.4. The measured low frequency noise characteristics is indeed a $1/f$ noise with a slope of ~ -1 in large area device (W/L = 5/10). The S_{ID} of large device is similar for different gate structures (Fig. 4(a)), but the S_{ID} of small device (W/L = 0.25/0.25) increases significantly in comparison to the S_{ID} of large device (Fig. 4(b)), and shows larger dependence on the gate structure due to the increase of STI edge effect. In Fig. 4(c), we can see that the value (f x S_{ID}) increases as frequency increases in small area device, but the value is nearly constant in large area device, which means the effects of the STI becomes significant as devices size decreases. In Fig. 4(d), the measured low frequency noise characteristics are similar to $1/f$ noise form in short channel device. The S_{ID}/I_D^2 characteristics of short channel devices are similar for different gate length (W/L = 0.25/0.2, 0.25/0.25, and 0.25/0.5), but the S_{ID}/I_D^2 characteristics of long channel devices (W/L = 0.25/3 and 0.25/10) increases significantly in comparison to the S_{ID}/I_D^2 of short channel devices and shows larger dependence on the gate length due to the increase of the STI edge effect. According to the data in Fig. 4, it seems that the interface state at the STI/channel interface affects the noise characteristics in high frequency range and is regarded as a kind of fast state.

4. Discussion

In narrow width devices, degradation of low frequency noise can be interpreted as the influence of interface state at the interface between channel and STI. We consider that the degradation of the device performance is due to the problem arising out of the etch process of the Si and oxide films in the STI process. The etch process can generate plasma damage and surface roughness on the sidewall of Si film. It seems that the BOX etch step of the STI process in SOI wafers increases the surface roughness and the interface-state. The etch process of Si film should be optimized especially in the devices with the narrow width to prevent the degradation of device performance and noise characteristics for analog-RF circuit applications

5. Conclusions

We have investigated the reason of low noise frequency degradation in narrow width SOI MOSFET with STI. As the channel width decreases, low frequency noise characteristics deteriorates due to the larger influence of the interface state which is caused by interface roughness. We have also analyzed the device characteristics with the gate shape (I-, T-, and H- shape in gate layout).

Acknowledgements

The authors would like to thank Dae-Gwan Kang, Chang-Yong Kanga t Hynix Semiconductor Ltd., Sang-Hyun Lee at SNU, and Jae-Gyung Ahn at IDT in USA. This work is supported by BK 21 and NRL .

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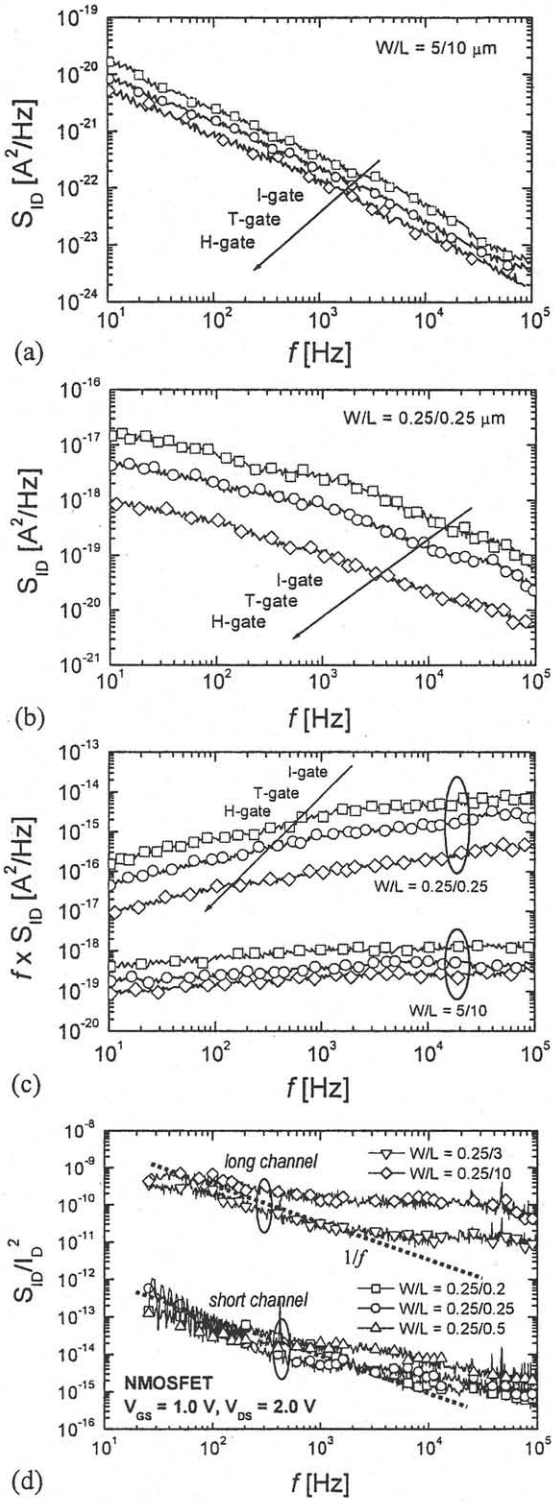

Fig. 4. I_{DS} noise characteristics for NMOSFETs at I_D = 20 μA, V_{DS} = 1.5 V. Noise power spectrum density of device with three different gate shape. (a) W/L = 5/10. (b) W/L = 0.25/0.25. (c) f x S_{id} versus frequency of W/L = 0.25/0.25 (upper site) and 5/10 (lower site) devices. (d) different device lengths of I-gate NMOSFETs at fixed device width (W = 0.25 μm).

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