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Key Issues for Manufacturable FeRAM Devices

Novel 0.35um FRAM Technology using Triple Level Aluminum Layer for High Speed and Low Voltage Operation

Tatsuya Yamazaki

FUJITSU Ltd., 4-2, Moriyama, Nishine, Kanegasaki-cho, Isawa-gun, Iwate 029-4593, Japan
Phone : +81-197-44-6650, Fax : +81-197-44-4846, #e-mail: yamazaki@unipro.ed.fujitsu.co.jp

In recent years, the progress of device technology for FRAM(TM) mass production fabrication has been remarkable. However, to increase the size of the available FRAM market, low voltage operation (less than 3V), high density package, high speed, and low cost are necessary.

In this study, we successfully developed a 256k bit FRAM device using a novel 0.35um technology. 3V operation was perfectly attained even with a doped PZT capacitor employed with triple level aluminum interconnect processes. In addition, a 47nsec access time at 3V was achieved, which definitely makes FRAM equivalent to SRAM devices. The whole process is fully compatible with conventional 0.35um high-end logic processes and design rules.

Figure 1 and **Figure 2** show cross section of our novel 0.35um device and top view of cell layout. **Figure 3** shows the cross sectional view of the actually fabricated device. The major process steps are summarized in **Table 1**. The underplaying CMOS structures are fabricated using current 0.35um logic processes without any specific change for subsequent FRAM formation processes. A thin encapsulation technique was employed to prevent process degradation caused by thermal budget and hydrogen species exposure in subsequent process steps. Followed by capacitor stack structure fabrication, first interlayer dielectric was deposited and fully planarized. The simultaneous high aspect ratio contact hole etching to S/D, polycide and bottom electrode was carried out. Then, deep via filling W-CVD and W-CMP were performed continuously. The structures between first level metal and third level metal were formed by conventional processes for logic device formation with W-via processes. Technology features are summarized in **Table 2.**

Figure 4 and **Figure 5** show a hysteresis loop and a Qtv curve, respectively, after capacitor fabrication from discrete capacitor (TE size: 50um x 50um). The Qsw above 30uC/cm2 was obtained even at 2V as shown in the Qtv curve, and Qsw was saturated at less than 3V. It is well-known that ferro performances are heavily deteriorated due to wiring processes after capacitor fabrication, and this is a big problem for device fabrication. To suppress capacitor degradation, we adopted an encapsulation technique. **Table 3** shows the comparison in ferroelectric performance after wafer processing with and without the encapsulation technique. Employing encapsulation, a Qsw value of more than 30uC/cm2 at 3V, and a V(90) of less than 3V, were achieved, and fatigue as well as retention performances were improved. The discrepancy between discrete and cell array capacitors was completely eliminated, which suggests that process degradation with cell array was improved by the encapsulation technique.

Using our novel 0.35um technology, we successfully integrated 2T/2C 256k FRAM, as shown in **Fig. 6.** The chip size is 14.8mm2, making it the smallest 256k FRAM in the worldwide to date. **Figure 7** shows the shmoo plot taken at 85C, indicating the relationship between chip enable access time (TCE) and VDD. It indicates that this device worked well with 47nsec even at 2.7V. This fact strongly indicates that the FRAM devices developed in this study have great potential to replace conventional SRAM devices with non-volatile storage.

In summary, we developed a novel 0.35um FRAM technology by employing a doped PZT capacitor and a special encapsulation technique. This process is fully compatible with conventional 0.35um high-end logic processes with triple level aluminum wiring. The 256k FRAM demonstrated in this study functioned at 85C with 47nsec even at 2.7V, which has FRAM superior to conventional SRAM.

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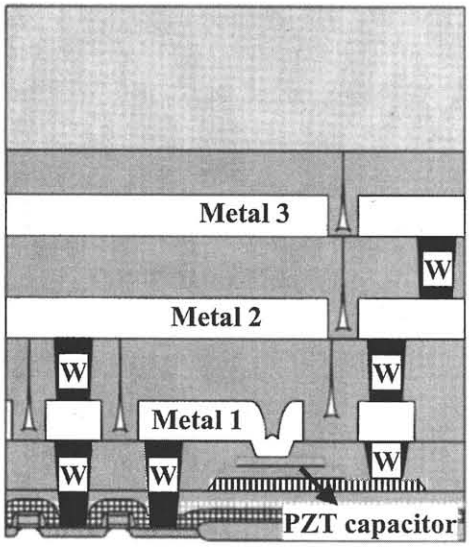

Fig. 1 Schematic diagram of cross section

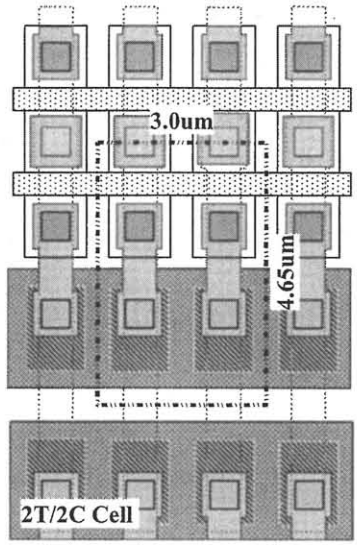

Fig. 2 Top view of 2T/2C cell layout
(Cell area : 13.95um2)

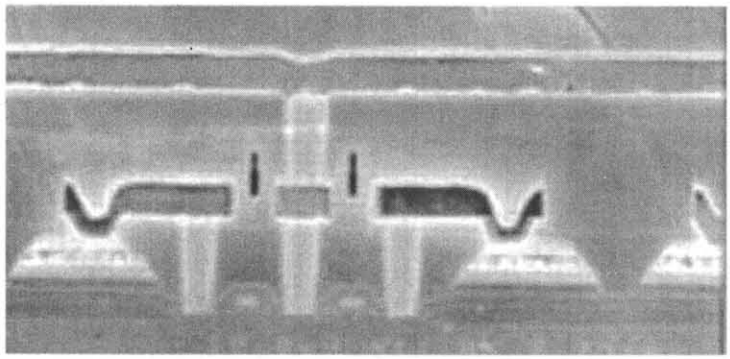

Fig. 3 Cross sectional view of fabricated device

Table 1 Major process steps

CMOS	Well Isolation
	Vth control
	Poly gate fabrication
	ILD CMP
FRAM	Ferro capacitor formation
	ILD CMP
	High aspect via etching
	W via filling + W-CMP
	Top electrode contact
	Recovery anneal
Triple Metal Wiring	First metal
	Second metal
	Third metal
	Passivation

Table 2 Technology features

Gate length	0.35um
Ferro capacitor	IrOx/PZT/Pt
S/D	TiSix
Via	W-plug
Metal	Triple aluminum
Metal pitch	1.1 um
Source voltage	3.0V
Cell size	13.95 um2 (2T/2C)
	8.69 um2 (1T/1C)

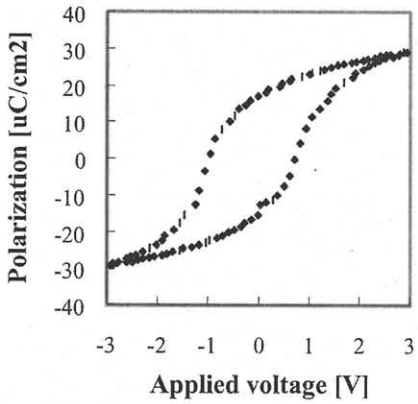

Fig. 4 Hysteresis loop after capacitor fabrication (50um x 50um)

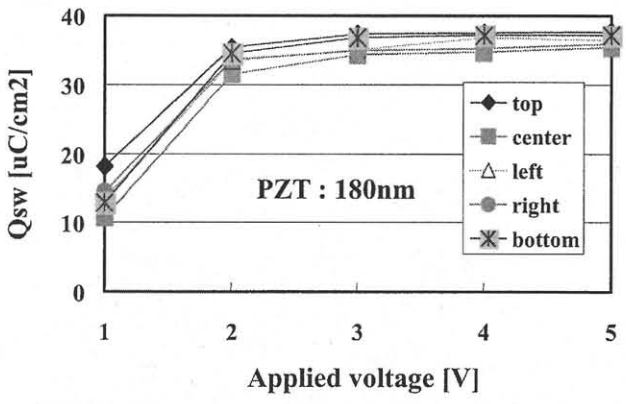

Fig. 5 Qtv curve after capacitor fabrication (50um x 50um)

Table 3 Comparison in ferro performance after wafer processing

	With encapsulation		Without encapsulation	
	Discrete	Cell array	Discrete	Cell array
Qsw at 3V	32uC/cm2	32uC/cm2	32uC/cm2	18uC/cm2
V(90)	2.2V	2.8V	2.2V	3.6V
Fatigue loss (5V, 1E9)	0%	7%	0%	12%
Imprint rate	-4%	-7%	-3%	-19%

Discrete: 50um x 50um
Cell array: 1.0um x 1.5um x 1660

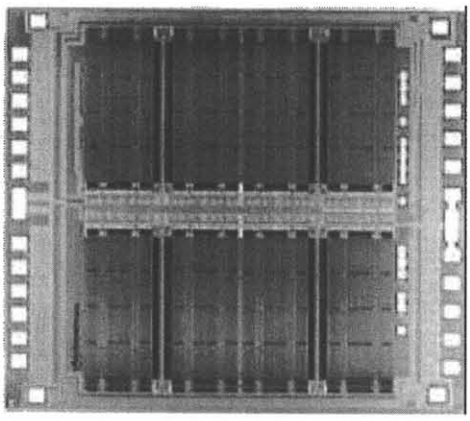

Fig. 6 Top view photograph of 256k bit FRAM (chip size 4.1mm x 3.6mm)

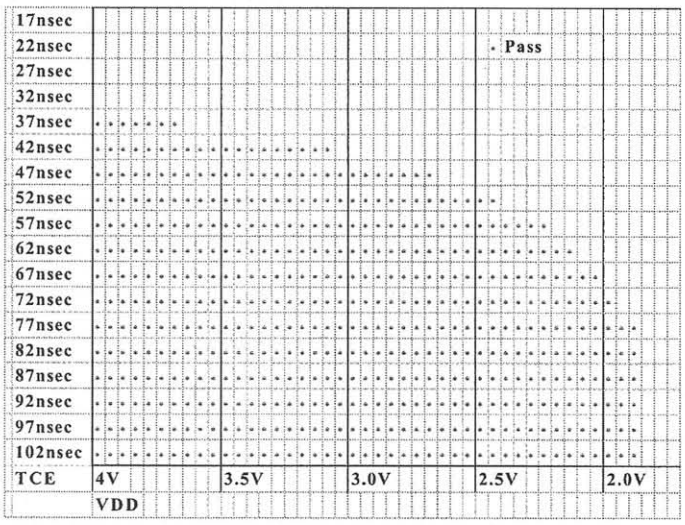

Fig. 7 Shmoo plot at 85 degree C.