Si-Dot Non-Volatile Memory Device

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Abstract
A Si-dot NVM device with program/erase (P/E) transients comparable to conventional stacked gate NVM devices, excellent endurance (>10^5 P/E cycles), and long-term non-volatility in spite of a thin bottom oxide (55-60Å) is presented. Its simple fabrication process makes this Si-dot NVM device a potential candidate for low cost embedded NVM applications.

Introduction
Unlike conventional floating gate NVM [1], Si-dot NVM devices rely on charge storage in a layer of discrete, Si-nanocrystals [2-4]. As compared to stacked-gate NVM, nanocrystal charge-storage offers several advantages: (1) low fabrication cost (single-poly); (2) better retention (Coulomb blockade and quantum confinement effects [5]), enabling tunnel oxides scaling and operating voltage reduction; (3) improved anti-punchthrough (no drain to floating gate coupling), allowing higher Vd, and shorter channel lengths; and (4) immunity to SILC and oxide defects b/o the distributed nature of the Si-dot charge storage.

Device Fabrication
_Nanocrystal layer fabrication_ Process cost and NVM performance are dependent on the physical properties of the Si-dot layer: dot size, dot size distribution, and Si-dot density; layer co-planarity and uniformity, and crystal-to-crystal interaction (lateral conduction). The desired layer Si-dot properties were achieved with a novel, three-step fabrication process [6,7]. (1) A Si aerosol is generated by the pyrolysis of diluted SiH4 at 950°C. Si-dots form by homogeneous gas-phase nucleation and grow by vapor deposition and coagulation. Process optimization resulted in the generation of spherical, single crystalline Si-dots (Fig. 1) with sub-3nm diameters. (2) A 1.5-2nm thermal oxide shell is grown at 1000°C on the particles to reduce crystal-to-crystal conduction in the Si-dot layer. The oxidation also sharpens the size distribution since the oxidation rate decreases with decreasing dot size [8] (Fig. 2). (3) A layer of Si-dots (density ~10^13 cm^-2) is thermophoretically deposited (temp delta = 200°C).

_NVM device fabrication_ This Si-dot process technique has been used to fabricate 0.2μm nMOS Si-dot NVM. A mono-layer of (oxidized) dots is deposited on a 4nm thermal oxide, and covered with a 8nm high-T oxide prior to poly-Si gate deposition.

Electrical Results
Drive current (30μA/μm), substrate slope (200mV/dec), and DIBL (100mV/V) values are typical for thick gate dielectric, high substrate doping NVM devices. Vt is defined as the gate voltage corresponding to a drain-source current of 1μA when a drain bias of 1V is applied.

Uniform FN tunneling has been used for both the program and the erase operation, though programming using channel hot-electron injection is possible as well. As is shown in Figs. 3 and 4, the high areal nanocrystal-density obtained by the aerosol fabrication process results in a large threshold voltage window (>2V), larger than those previously reported on nanocrystal devices [4,9]. This large Vt, window results in a high read-out current (20μA/μm for gate and drain biases of 2.5V and 1V, respectively), allowing fast memory access. The transients further illustrate the voltage/performance trade-off for this device, and show that in spite of the low gate coupling ratio (inherent to Si-dot NVM) μs programming and ms erasure is possible at moderate operating voltages.

Further, excellent endurance characteristics are observed on the Si-dot NVM device; limited window closure is measured after 5x10^5 P/E cycles (Fig. 5). The gradual shift of the Vt window to voltages indicates fixed charge build-up in the gate oxide layer. Disturb and retention data before and after cycling are presented in Figs. 6 and 7, and Fig. 8, respectively. In spite of the thin tunnel oxide, reasonable disturb times and long data retention is obtained, indicative of the intrinsic advantages of discrete charge storage. Further optimization of the gate dielectric stack is necessary, however, in order to claim non-volatility. No SILC has been observed. In addition, no drain disturb was detected, even at drain voltages as high as 4V, which indicates that there is no or only limited lateral conduction in the nanocrystal layer (Fig. 6).

Conclusions
A Si-dot floating-gate NVM has been fabricated based on a low cost process. A new, aerosol-based technique has been used to integrate a very dense (10^13 cm^-2), co-planar, and uniform layer of spherical, single-crystalline Si-dots in the gate dielectric of 0.2μm nMOS devices. These devices demonstrate good electrical characteristics, including high Fn, promising disturb behavior, excellent endurance, the absence of SILC, and long-term charge retention after cycling.
Fig. 1: Planar view of an aerosol Si-dot monolayer. Dot size is 4-5nm and dot density is $6\times10^{12}$. Crystallinity and spherical shape of the Si-dots can be seen in the inset (from a different sample with 13nm particles).

Fig. 2: Size distribution of two different aerosols, one with an average S-dot diameter of 7.3nm, the other with an average diameter of 13nm.

Fig. 3: Programming transients (uniform FN tunneling) of the Si-dot NVM device. The device programs to a high $V_t$ of $+3.3V$ in 50$\mu$s with gate and substrate bias of $+8V$ and $-5V$, respectively.

Fig. 4: Erase transients (uniform FN tunneling). The device erases to a low $V_t$ of $+1V$ in 100ms with gate and substrate bias of $+7V$ and $-8V$, respectively.

Fig. 5: Endurance characteristic; only limited window closure is observed after $10^5$ program/erase cycles. The shift to higher voltages signals the build-up of fixed charge in the gate dielectric stack.

Fig. 6: Gate and drain disturb characteristics. Zero bias is applied to all nodes except for the node mentioned in the legend, i.e. either the gate ($V_g$) or the drain ($V_d$).

Fig. 7: Gate disturb characteristics. A negative bias is applied to the gate while all other nodes are kept grounded.

Fig. 8: After cycling, long room-temperature non-volatility is observed under both retention and read-out conditions (note: the intrinsic $V_t$ is approximately 3V).

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