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Novel Capacitor Technology for Sub-Quarter Micron 1T1C FRAM

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1. Introduction

Ferroelectric random access memory (FRAM) has been attracted in recent decades due to its ideal memory properties such as non-volatility, fast access time and low power consumption [1]. In order to fully utilize the ideal memory properties, it is prerequisite to develop high density FRAM device, which demands 1 transistor 1 capacitor (1T1C) cell architecture and capacitor over bitline (COB) cell structure. Recently, we developed 1T1C 4Mb FRAM device using 0.6 μm design rule and COB structure [2]. However, the 4Mb FRAM device cannot satisfactorily be used as major memory device for stand-alone application due to its low density and cost ineffectiveness. Therefore, it is strongly required to develop high density FRAM device beyond 32Mb with 0.25 μm design rule for productworthy stand-alone memory devices. In the 0.25 μm design rule, the space margin between the ferroelectric capacitors is drastically reduced from 0.8 μm to 0.3 μm as shown in Figure 1 a), which describes the trend of space margins as a function of design rule. In order to satisfy the tight drawn space margin, highly steep etching slope of 85° should be achieved for current ferroelectric capacitor stack with total thickness of 7500Å. Unfortunately, current etching technology is not mature enough to provide the required high etching slope due to the difficulty in etching novel electrode metals such as Ir and Pt. Figure 1 b) shows the maximum allowable stack height for given etching slope. Considering the limitation of current etching slope of 70 °, the capacitor stack height should be reduced from current 7500Å to 4000Å for developing 0.25 μm FRAM technology.

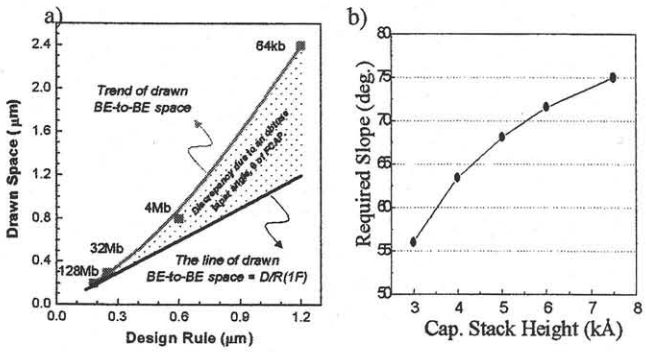

Fig. 1 a) Capacitors node separation as a function of design rule, b) the dependence of maximum stack height on etching slope.

In order to produce the 4k capacitor stack, the thickness of sol-gel derived $Pb(Zr_{1-x}Ti_x)O_3$ (PZT) films was greatly reduced from 2000Å to 1000Å. The thickness reduction was accomplished by using $PbTiO_3$ (PTO) seeding layer and optimal PZT composition, which also make it possible to anneal the PZT films at a low temperature of 600 °C. In addition, as the PZT thickness decreases further, the effect of interface becomes more pronounced. It is well-known that the interface between PZT films and top electrode plays dominant role in degrading ferroelectric capacitors during integration. Therefore, in order to develop robust 4k stack capacitor, it is required to minimize the harmful interface effect. In this experiment, the interface effect was completely minimized by enhancing the heat-treatment of top electrode at 650 °C using rapid thermal process (RTP).

In this paper, we successfully developed highly stable 4k capacitor stack by using seeding layer, optimum PZT composition, and high temperature top electrode annealing. The feasibility of ultra thin 4k capacitor stack using 1000Å thick PZT films was for the first time evaluated and confirmed in real functional device level.

2. Experimental Technique

$Pt/IrO_2/Ir$ bottom electrodes are deposited on poly-plugged substrate by using DC sputtering technique. The 4k stack capacitor is composed of 1000Å thick Pt, 300Å thick IrO_2, and 500Å thick Ir. The sol-gel derived PTO films were first prepared on $Pt/IrO_2/Ir$ poly-plugged substrate as a seeding layer, and then the PZT films were spin-coated on the as-deposited PTO films by using sol-gel technique. The PZT/PTO films were annealed at a low temperature of 600 °C for 1 min in O_2 atmosphere. Top electrode IrO_2 films with thickness 200Å were then sputter-deposited on the polycrystalline PZT films, and annealed by two different methods. One is conventional furnace annealing at 450 °C for 30 min in O_2 atmosphere. The other is rapid thermal process annealing at 650 °C for 1 min in O_2 atmosphere for enhancing the interface between PZT films and top IrO_2. After the top IrO_2 annealing, 1000Å thick Ir electrode was sputter-deposited on the IrO_2 films. After the ferroelectric capacitor formation, each electrode was etched by using three different photo masks. After patterning the ferroelectric capacitor stack, atmosphere pressure chemical vapor deposition (APCVD) oxides are prepared as interlayer dielectric (ILD) material over the patterned ferroelectric stack, and then via contact was generated on the ILD oxide. Aluminum metal line was finally prepared and dry-etched for electrical evaluation.

3. Results

Figure 2 shows the phase formation and surface

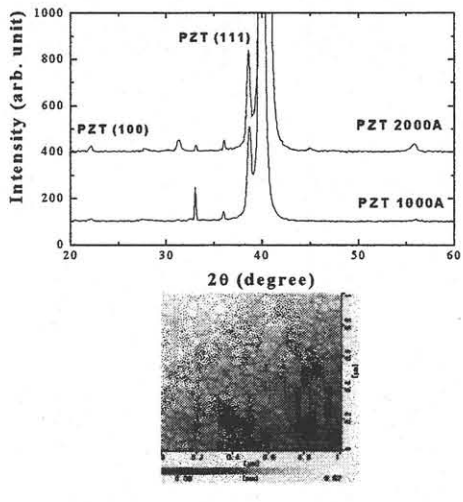

Fig. 2 a) XRD patterns for PZT films with thickness of 2000Å and 10 00Å, respectively, b) AFM image of 1000Å PZT films.

morphology of 1000Å PZT films on Pt 1000Å/IrO_2 300Å/Ir 500Å substrate. It was observed that the polycrystalline PZT films displayed highly (111) orientation without any presence of pyrochlore phase. The pure perovskite phase formation at a low annealing temperature of 600 °C might be attributed to the PTO seeding layer, which provides nucleation sites and thus reduces the phase formation energy. The PZT films also illustrate very smooth surface morphology with fine grain size in which no pyrochlore phase was found.

Figure 3 shows the Q-V curves of 4k stack and 7k stack capacitors after completing full integration process. It was observed that the 4k stack capacitors show steeper Q-V curve than the 7k stack capacitors with 2000Å thick PZT films, which was attributed to high electric field on the 1k PZT films. By drawing the loadline in the Q-V curve, the 4k stack exhibited larger switching and non-switching charges than the 7k stack capacitors, which means that the 4k stack capacitors display larger data "1" and "0" charges at a operating voltage of 3.3V than the 7k stack. We also evaluated the Q-V curves for two different 4k capacitors whose top electrodes were annealed by furnace at 450 °C or by RTP at 650 °C. It was found that very poor ferroelectric properties were obtained for the 4k capacitors by conventional furnace top electrode annealing at 450 °C. On the other hand, the low stack capacitors by RTP top electrode annealing at 650 °C show the excellent Q-V curve, which means that the RTP top electrode annealing process completely minimizes the harmful interface effect induced by the integration process.

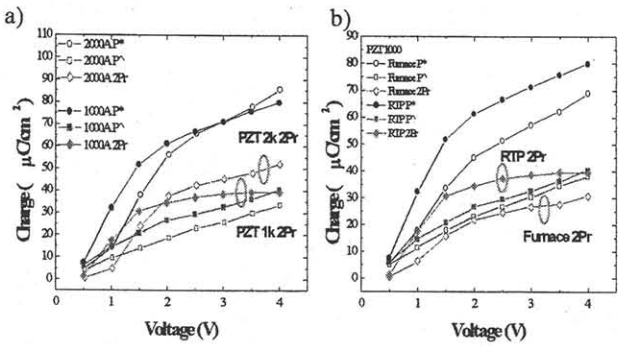

Fig. 3 a) Q-V curves of a) PZT films with thickness of 2000Å and 1000Å, b) 1000Å thick PZT films processed with top electrode annealing by furnace at 450 °C or by RTP at 650 °C.

Figure 4 shows the cross-sectional scanning electron microscopy (SEM) pictures after full integration process. The 4k capacitor stack was successfully fabricated in 4Mb FRAM vehicle without any process issues. Compared to conventional 7k capacitor stack, the 4k thick capacitors generates stable ILD and IMD backend process due to its low stack height.

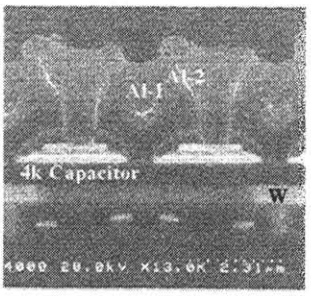

Fig. 4 Cross-sectional SEM image after full integration

Since the thickness of diffusion barrier layers was drastically reduced from 1500Å to 500Å in the 4k stack capacitor, it is necessary to evaluate the variation of buried contact (BC) resistance. Figure 5 shows the distribution BC resistance for 4k stack capacitors and current 7k stack height, respectively. It was observed that the 4k stack displayed average value of 900 ohm per contact, which is quite comparable to that of 7k stack capacitor. The low BC resistance was achieved by lowering PZT crystallization temperature from 700 °C to 600 °C, which results from PTO seeding layer and Ti-rich PZT composition.

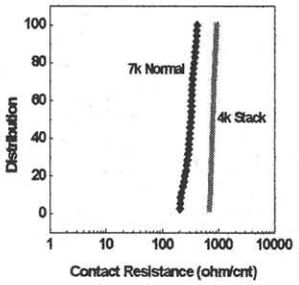

Fig. 5 BC resistance of 7k stack and 4k stack

Figure 6 shows the charge distribution of 4M cells prepared by conventional ferroelectric capacitors and the low stack capacitors, respectively. The charge distributions of data "1" and data "0" were shifted upward for the 4k stack capacitor. As observed in Q-V curve, since the 4k capacitor shows very steep rise, the large switching charge of data "1" is generated for the 4k capacitor. From the wide sensing window, fully working 4Mb chip using the 4k capacitor was successfully achieved.

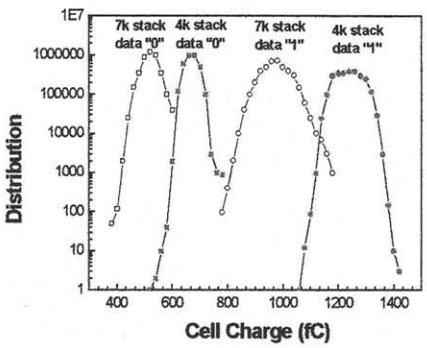

Fig. 6 Charge distribution of 7k stack and 4k stack

4. Summary

Using the PTO seeding layer, Ti-rich PZT films, and high temperature top electrode annealing, it was possible to develop robust 4k ferroelectric capacitor stack for high density FRAM device beyond 32Mb with 0.25 μm design rule. The feasibility of 32Mb capacitor module was confirmed by implementing the low stack capacitor into 4Mb FRAM vehicle. The ferroelectric capacitors exhibited average data "1" charge and data "0" charge of 1200 fC and 620 fC, respectively, which are highly comparable to that of 4Mb FRAM. Therefore, this feasibility clearly demonstrates strong possibility of producing high density 32Mb FRAM device with 0.25 μm design rule.

References

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[2]S.Y. Lee, D.J. Jung, Y.J. Song, B.J. Koo, S.O. Park, H.J. Cho, S.J. Oh, D.S. Hwang, S.I. Lee, J.K. Lee, Y.S. Park, I.S. Jung, and K.N. Kim, VLSI Tech. Symp., (1999) p.141.