

C-8-3

Modeling of Polarization Relaxation Effects in Ferroelectric Memory^(a,b)C.W.Tsai, ^(b)S.Y. Lee, ^(a)S.L. Lung, ^(a,b)T. Wang^(a)Macronix International Co.^(b)Dept. of Electronics Engineering, National Chiao-Tung University
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Abstract

A SPICE compatible polarization relaxation model for ferroelectric memory has been developed. An excellent fit to measured result is obtained. The sense voltage in a 2T/2C cell is significantly reduced from the relaxation model. The relaxation effect on minimum sense voltage attributed to capacitance mismatch in a 1T/1C cell is also evaluated.

Introduction

Ferroelectric random access memory (FeRAM) has received much interest due to shorter access time, lower dynamic power consumption and higher write endurance than floating gate non-volatile memories such as EEPROM and Flash. However, some reliability issues can still lead to a failure of the memory cells [1,2]. Polarization relaxation is one of these effects, which is referred to as a fast-decaying component that degrades the sense margin between the switching and non-switching levels bilaterally [1]. Various kinds of modeling methods have been proposed for ferroelectric capacitors in the past decade [3]. Most of them are based on the measured P-E hysteresis loop. These models lack of the ability of simulating relaxation effect and tend to overestimate the amount of available charge. In this work, a SPICE compatible ferroelectric capacitor model with relaxation effect is proposed. The transient behavior of a FeRAM cell can be well predicted by this model.

FeRAM Capacitor Characterization

Pulse measurement is performed by using a $2000\mu\text{m}^2$ Pt/PZT(sputtered)/IrO_x capacitor. A capacitor of 1nF and a resistor of 82Ω are used in P-E and I-t measurements, respectively.

Modeling of Polarization Relaxation

The polarization relaxation effect manifests itself by a gap in a single loop P-E measurement (Fig.1). Fig.2 compares the hysteresis loop simulated by a conventional non-relaxation model [3] and measured result. A circle in Fig. 2 highlights the discrepancy. The conventional model ignores the relaxation component and may exaggerate the sense voltage in a FeRAM cell.

Incorporation of the relaxation effect with a conventional model can be realized by means of connecting a relaxation voltage source via a linear capacitor as shown in Fig.3. The circuit diagram of the relaxation voltage

source is drawn in Fig. 4. The voltage source constructed in Fig.4 can send a pull-up/down voltage signal with $\log(t)$ dependence to simulate the evolution of polarization (Fig. 5). The decaying rate of the relaxed component is extracted from measurement data.

Results and Discussion

The pulse response in Fig. 5 depicts the fast-decaying relaxation component. Good agreement between modeling and measurement is achieved. The relaxation component exhibits logarithmic time-dependence [4]. Fig. 6 shows simulated and measured single cycle hysteresis loops. The proposed model can precisely simulate the relaxation of polarization, i.e., the discontinuity in the loop. The measured and simulated I-t (C_{ferro} in series with a resistive load) characteristics are plotted in Fig. 7. The simulated relaxation transient agrees with the measured result in each of switching and non-switching cases.

The model is used to evaluate the impact of relaxation on the sense voltage in a 2T/2C cell. The result is shown in Fig. 8. The sense voltage is reduced considerably as relaxation time increases. The result from a conventional model is also shown in the figure. In Fig. 9, we evaluate the relaxation effect on minimum sense voltage required in a 1T/1C cell due to capacitance imbalance. The capacitance mismatch may arise from inherent degradation such as imprint [2] or process variations. The simulated minimum sense voltage is shown in Fig. 9(b). It should be noted that, unlike the result in Fig. 8, the worst case occurs when polarization is not relaxed at all.

Conclusion

We have developed a ferroelectric capacitor model including polarization relaxation. Our study indicates that the relaxation of polarization may have opposite effects in different issues. In order to achieve an accurate FeRAM design, circuit simulation taking into account the relaxation effect is necessary.

- [1] R. Moazzami et al., Symp. VLSI Technology, p.61, 1991
- [2] S. Tanaka et al., IEEE Trans. Electron Dev., p.781, 2000
- [3] A. Sheikholeslami et al., IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control, p.917, 1997
- [4] J. M. Benedetto et al., J.Appl.Phys., p.464, 199

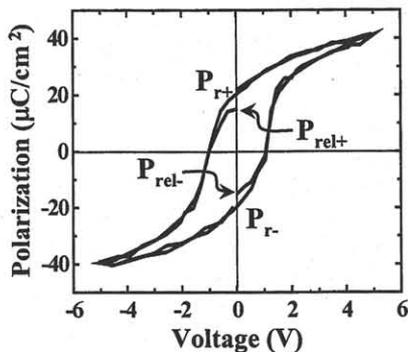


Fig. 1 Positive and negative single loop measurement result exhibiting a relaxation component at each polarity. P_r and P_{rel} refer to the remanent and non-volatile remanent polarization.

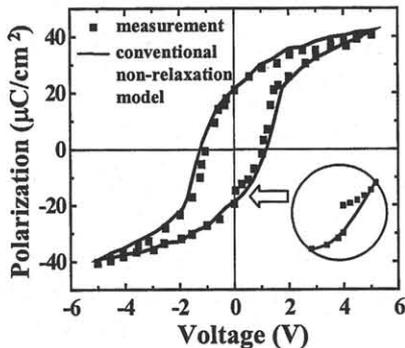


Fig. 2 Hysteresis loop simulated by a conventional model. The circle highlights the difference between the model and the measurement data.

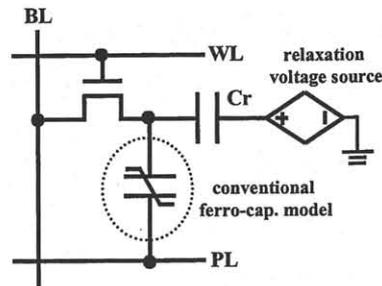


Fig. 3 Schematic diagram of a conventional ferroelectric capacitor model combined with a relaxation source. C_r is chosen to be far below the value of bit-line capacitance.

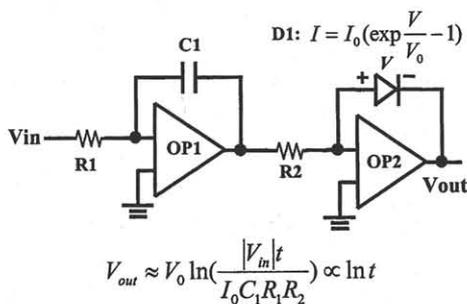


Fig. 4 Schematic diagram of the relaxation voltage source used in Fig. 3. $V_{out}(t)$ follows a logarithmic time dependence. All parameters in this circuit are chosen to fit the relaxation rate from experiment.

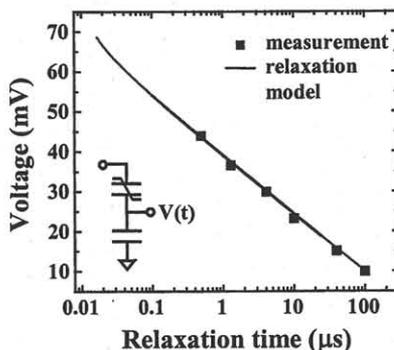


Fig. 5 Measured and simulated pulse responses with a capacitive load which depicts a fast-decaying relaxation component after trail edge.

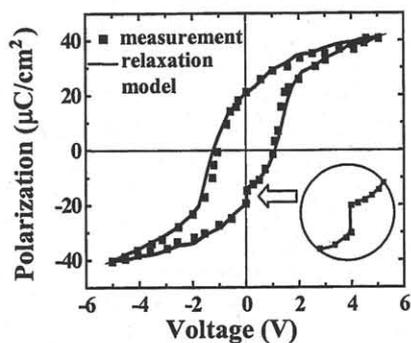


Fig. 6 The measured and simulated P-V curves.

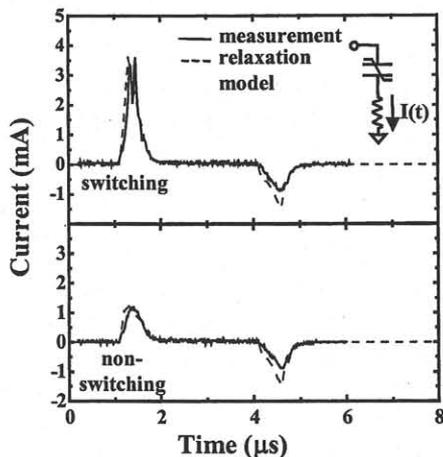


Fig. 7 The measured and simulated I-t curves.

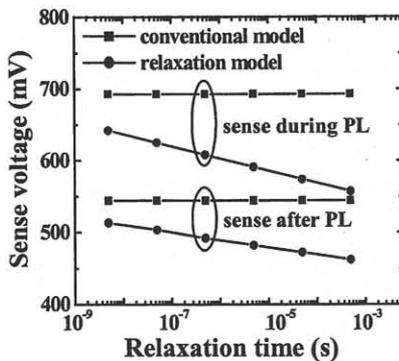


Fig. 8 The simulated bitline sense voltage versus elapsed time since the last cell access.

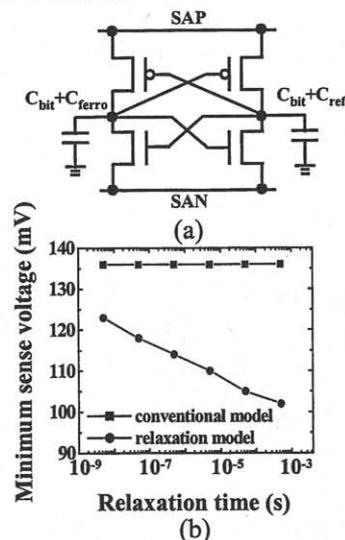


Fig. 9 (a) Sense amplifier with capacitance imbalance. (b) Minimum sense voltage versus relaxation time after PL pulse. The cell capacitor is assumed to be imprinted (0.5V shift) towards the positive voltage direction.