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Improved Retention Characteristics of Metal-Ferroelectric-Insulator-Semiconductor Structure Using a Post-Oxygen Annealing Treatment

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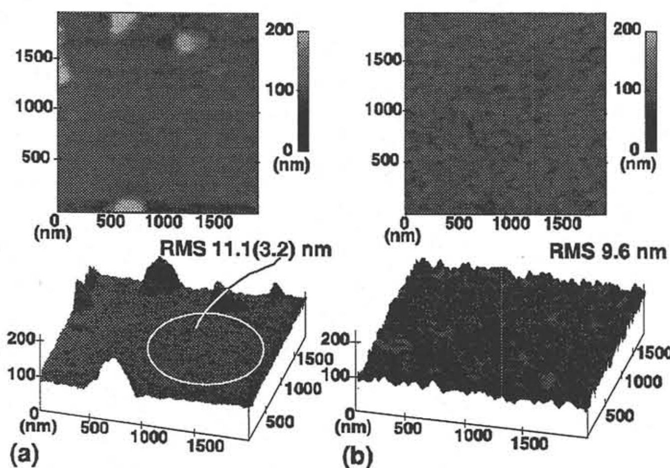
1. Introduction

MF(M)IS(Metal-Ferroelectric-(Metal-)Insulator-Semiconductor) structures have been attracting much attention as candidates for practical use in FET-type nonvolatile memories with nondestructive readout operation, which follow a good scaling-down rule. However, many MFS and MF(M)IS FET memories have still short retention times except for a few successes [1, 2]. We have studied those retention degradations of MFIS structures theoretically, which is affected significantly by M/S interface and property of ferroelectric layer. From the analysis, current flow through the ferroelectric degrade the retention characteristics[3,4].

In this work, improvement of retention characteristics of MFIS structures has been experimentally tried by obtaining good quality of the M/S interface and the ferroelectric film. Very long retention time has been obtained by post-O_2 annealing.

2. Experimental

$SrBi_2Ta_2O_9$(SBT) thin films were used as the ferroelectric layer, which were deposited on Pt/Ti/SiO_2/Si(100) and SiON/n-Si(100) substrates at 550°C in O_2 atmosphere by PLD method by using a stoichiometric SBT ceramic target[5]. Several MFM (Metal- Ferroelectric-Metal) and MFIS structures were annealed at 600°C in O_2 atmosphere for 20 minutes. The others were left as-deposited. Finally top electrodes of 250μmϕ were formed on the SBT.



Figs.1. AFM surface images of (a) as-deposited SBT and (b) annealed SBT films.

3. Results and Discussion

AFM images of SBT/SiON/Si surface are shown in Figs.1(a),(b). Hillocks on the smooth SBT surface are observed for the as-deposited samples (Fig.1(a)). Only smooth areas have exhibited average roughness(RMS) of 3.2nm, which has been estimated as 11.1 nm if the hillocks will be taken into account. After annealed, the RMS has been reduced to 9.6 nm. The hillocks shown in Fig.1(a) have disappeared and the surface has been covered by uniform-sized SBT grains as large as 80 nm (Fig.1(b)). Roughness of SBT surface is considered to induce leakage current into the layer, which will severely degrade the retention characteristics.

XRD patterns of Fig.2 show that the annealed sample has a higher SBT(105) peak than the as-deposited. Almost the same crystal structures have been obtained for the two samples.

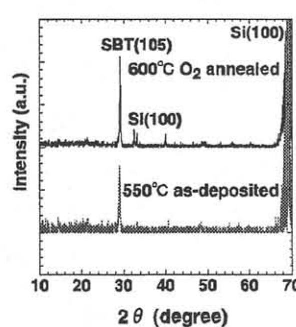


Fig.2. XRD patterns of SBT films.

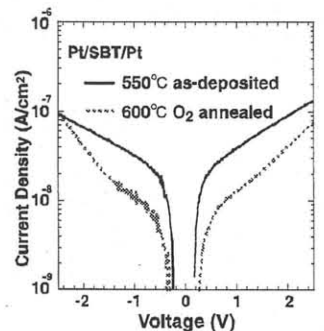
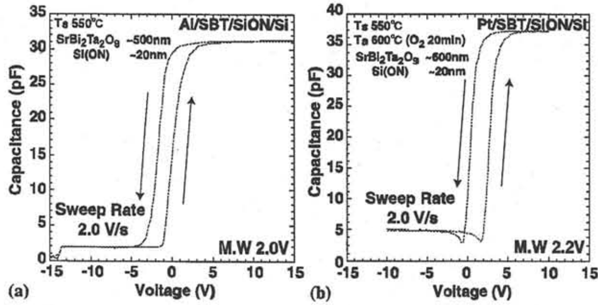
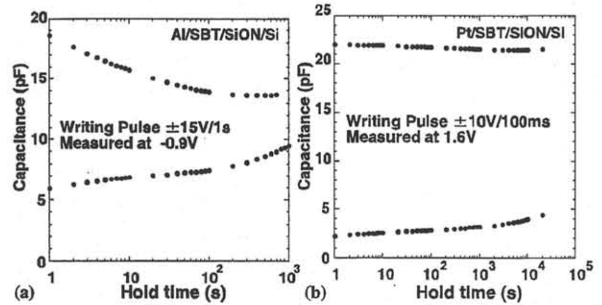


Fig.3. I-V characteristics of MFM capacitors.



Figs.4. C-V characteristics of MFIS structures using (a) as-deposited SBT and (b) annealed SBT films.



Figs.5. Retention characteristics of MFIS structures using (a) as-deposited SBT and (b) annealed SBT films.

I-V characteristics of two Pt/SBT/Pt capacitors for an as-deposited and an annealed SBT films have been investigated (Fig.3). The annealed sample has shown much less current density by about a half of order of magnitude than the as-deposited, especially in low field. We assume the two main reasons for this improvement of the I-V characteristics. One is the disappearance of hillocks on SBT surface by annealing as discussed above. The other is decrease of oxygen vacancies in the SBT layer by O_2 annealing gas, which can lead charge conduction in the layer. A further study has been done on the conduction processes, which have been analyzed by using a following equation:

$$J = J_{Sk} + J_{FP}$$
$$= aT^2 \cdot \left\{ \exp\left(+b\frac{\sqrt{V}}{T} - \frac{q\phi_B}{kT} \right) - 1 \right\} + cV \cdot \exp\left(+2b\frac{\sqrt{V}}{T} - \frac{q\phi_B}{kT} \right), \quad (1)$$

where a, b and c are positive constants, k Boltzmann constant, T temperature, and ϕ_B barrier height, respectively. The calculated contribution of Schottky emission J_{Sk} has shown much decrease after annealed, although that of Frenkel-Poole emission J_{FP} has not seemed to be sensitive to the annealing treatment. The analysis has indicated that the annealing has affected mainly SBT surface. About 25 meV increase of the surface barrier height has been estimated.

C-V hysteresis loops for an as-deposited Al/SBT/SiON/Si (Fig.4(a)) and an annealed Pt/SBT/SiON/Si (Fig.4(b)) have been measured. The loop for the as-deposited MFIS has shown a amall negative voltage shift. The as-deposited sample has shown a memory window of 2.0V at sweeping voltage from –15V to +15V (Fig.4(a)). The annealed sample, on the other hand, has shown little voltage shift with a memory window of 2.2V at sweeping voltage from –10V to +10V (Fig.4(b)). This result means that the annealed MFIS can be operated by lower voltage than the as-deposited, meaning lower leakage through the MFIS and better squareness in SBT hysteresis than the as-deposited.

Retention characteristics have been studied for these two MFIS structures (Figs.5(a),(b)). The writing conditions have been decided to obtain saturated hysteresis loops. DC bias voltages have been applied. In spite of lower writing pulse amplitude (+-10V) and short pulse time(100ms), compared to those for as-deposited (+-15V, 1s), the annealed MFIS has shown the retention time of 2×10^4 s or more which is much longer retention time than the as-deposited.

4. Summary

Post annealing at 600℃ in O_2 atmosphere has been performed in order to improve the retention characteristics of MFIS structures. In the case of MFM structure, the annealing treatment has less roughness of the SBT surface, contributed to its crystallization, and reduced leakage current effectively through the structure. These phenomena are thought to contribute greatly the improvement of retention characteristics of MFIS structure for ferroelectric nonvolatile 1T-type memory.

Acknowledgment

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