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Advantage of a Quasi-Nonvolatile Memory with Ultra Thin Oxide

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Abstract— **To realize random accessible storage device, we propose a sub-0.1 μm floating gate memory that uses direct tunneling for low voltage operations (applied word line voltage $\leq$ 6 V, bit line voltage $\leq$ 2V). Although the memory has very leaky oxide barrier (2.5 nm), its new structure achieves long retention time. We have discussed the random accessibility from memory cell properties.**

I. Introduction

Flash memory is coming to its scaling limit due to the high operation voltage, and it has complex write/erase operation. To overcome these problems, we proposed and demonstrated a novel Floating Gate (FG) memory, Direct Tunneling Memory (DTM) [1], [2]. The features of DTM are ultra thin direct tunneling oxide, simple random access at low voltage, and fully compatible fabrication with that of MOSFET. Due to these features, DTM is suitable not only for break-through of the scaling limit but for embedded memory application.

This paper demonstrates the longer retention time and the larger V_{TH} shift for improved DTM with a new FG structure. Furthermore we show writing characteristics of DTM and discuss its random accessibility.

II. DTM Structure

The key to success of DTM is suppression of the leakage current through thin tunneling oxide. Both the self-aligned sidewall Control Gate (CG) and the leakage stop barrier have prevented the leakage process [1]. However, DTM requires higher performance to be launched into a real market.

Figure 1(a) shows the improved structure of DTM, where FG length is about 60 nm. We introduce a FG depletion region at the thin tunneling oxide interface. This depletion region, which is fabricated by a diffusion stopper, suppresses not only the thermally excited leakage current by enhancement of the leakage stop barrier, but the interface state assisted leakage current [3] by removing FG electrons from tunneling oxide interface (Fig. 1(b)).

Most of fabrication steps are same with those in Ref. [1]. Major differences are no FG protect layer, insertion of the diffusion stopper (chemical oxide) in FG by HNO_3 treatment, and As+ implantation for FG.

III. Memory Cell Performance

We show the retention characteristics: threshold voltage (V_{TH}) shift in Fig. 2. Here, a high (low) V_{TH} is called a "0" ("1") state, and we try to set that a minimum "0" level (maximum "1" level) is 1.2 V (0.8V). The retention time of the improved DTM is longer, and its V_{TH} shift is about twice as wide as an old one [1], [2].

Figure 3 plots write characteristics for pulse widths of a word line voltage V_{WL} which is applied to CG of DTM. Obviously, the writing "1" speed is comparable with the writing "0" speed.

We also investigate writing characteristics from several initial V_{TH} levels. When "0" write pulse (V_{WL}= 6V) width is 30 μsec, V_{TH} levels are over the minimum "0" level. The level shifts from any initial V_{TH} have a same pulse dependence > 30 μsec. For "1" write pulse, the level shifts also show a convergency (> 70 μsec), and then 100 μsec pulse V_{WL} can suppress V_{TH} under the maximum "1" level even if an initial V_{TH} is enough high.

IV. Cell Array Operation

These convergence properties certainly make "0"/"1" state on a DTM cell. Then DTM array will be operated along a simple three-steps flow as shown in Fig. 4(a). Figure 4(b) shows "AND type" cell array. ("NOR type" array can be also designed for DTM.)

There exist two disturbances "Type A" and "Type B" for the writing "0" (see Fig. 4(b)), and these properties shows Figs. 5 and 6. For Type A, DTM cell can remain "1" state even if we apply V_{WL}= 6V for 200μsec. A cell of Type B shows only 40 m eV drop of "0" state for 10^4 sec. Therefore, the operation of the writing "0" has enough margins for the disturbances.

V. Conclusion

We can operate DTM with low voltage. Especially, maximum V_{BL} is only 2V. Therefore DTM has a distinct advantage of reducing the cell size. Due to both the convergency of V_{TH} shifts and the fast "1" writing, DTM may realize the random access memory. Then the writing operation will be easier and faster than Flash memory. Furthermore, the DTM cell has the extremely high endurance for 10^9 times rewriting. Then, it enables a system frequently to swap a lot of data.

DTM has the above advantages in exchange for a data nonvolatility, and its quasi nonvolatility needs the refresh operation for a data retention. However, standby power consumption will be extremely low ($\leq$ 1 μW), because a refresh period is much longer than 1 day (see Fig. 2). Consequently, DTM can be used as a storage RAM.

References

[1] N. Horiguchi, *et. al.*, *IEDM 99*, p.922.
[2] T. Usuki *et. al.*, *Silicon Nanoelectronics Workshop 2000*, p. 83
[3] A. Ghetti *et. al.*, *IEDM 99*, p. 723.

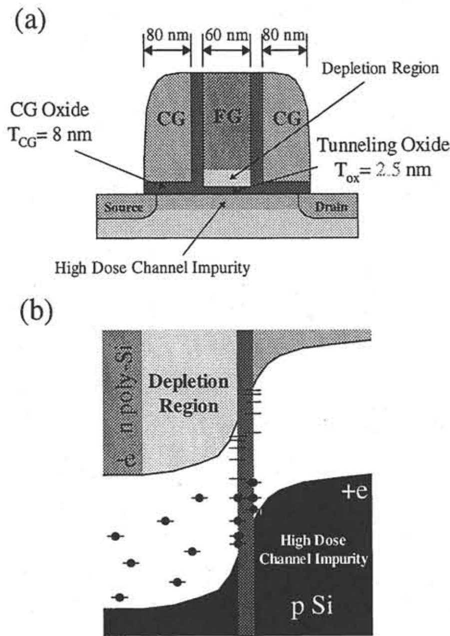

Fig. 1. (a) Cross-section of DTM. (b) Band diagram at tunneling oxide interface. The FG depletion region enhances the built-in potential between n+ FG and channel, and it removes FG electrons from the tunneling oxide interface.

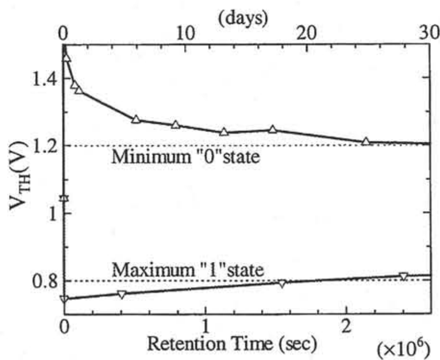

Fig. 2. DTM retention characteristics.

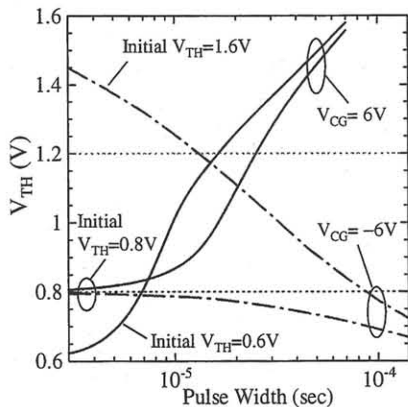

Fig. 3. Writing "0","1" characteristics. Convergency for write operation enables random access.

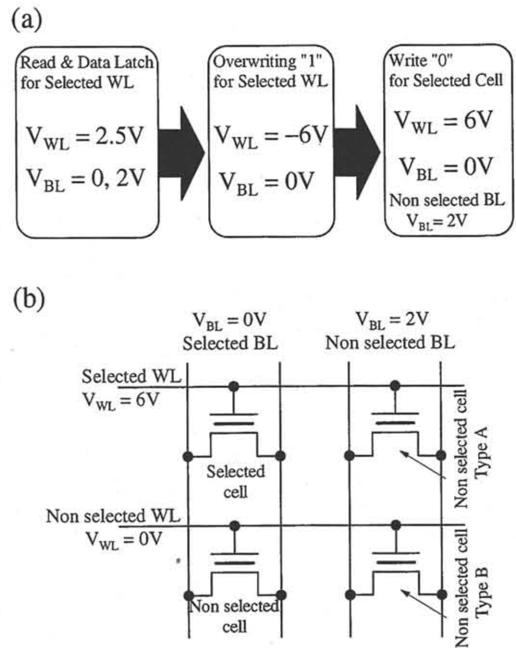

Fig. 4. (a) Operation flow of write mode. (b) AND type array for writing "0."

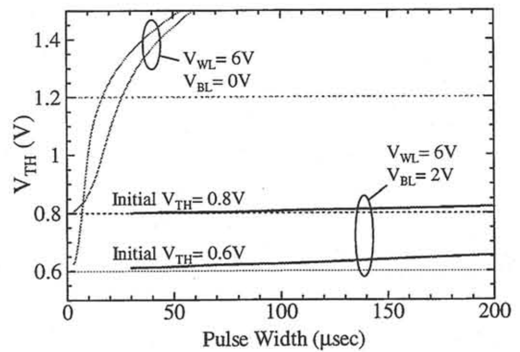

Fig. 5. Disturbance for non selected cell (Type A). This cell can remain "0" state even if we apply $V_{WL}= \pm 6$V for 200μsec.

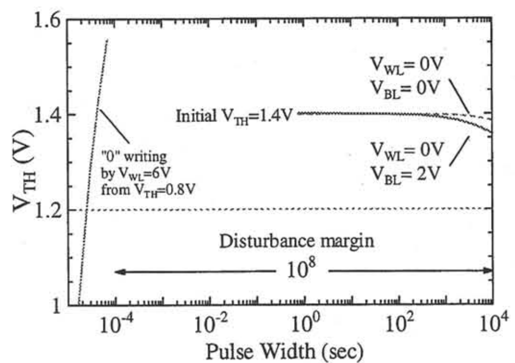

Fig. 6. Disturbance for non selected cell (Type B). There is an enough large margin for the disturbance.