C-9-3

Electron Discharge Model of Locally-Trapped Charge in Oxide-Nitride-Oxide (ONO) Gates for NROMTM Non-Volatile Semiconductor Memory Devices

Eli Lusky, Yosi Shacham-Diamand⁽¹⁾, Ilan Bloom⁽²⁾ Boaz Eitan⁽²⁾

Ph.D Student, Tel-Aviv University, Dept. of Physical Electronics, Ramat Aviv, 79978 Israel

Phone: 972-9-8850830-242, Fax:972-9-8850831, E-mail:elusky@saifun.com

⁽¹⁾ Tel Aviv University, Dept. of Physical Electronics, Ramat Aviv, 79978 Israel

⁽²⁾ Saifun Semiconductors Ltd., 14 Hamelacha st., Ind. Zone South, P.O.Box 8385, Netanya, 42504 Israel

1. Introduction

The information in conventional non-volatile semiconductor memory devices is stored as a charge in a conductive floating gate [1], or in an insulating layer such as in MNOS and SONOS [2] devices. In both cases there is homogeneously charge distribution over the channel region. The NROMTM non-volatile memory device [3] is a novel two-bit memory cell based on localized trapped-charge in a nitride layer covered by thick top-oxide (7 nm) and bottom-oxide (9 nm). In this work we present an electron discharge model of the localized-trapped charge in an NROMTM non-volatile memory device.

Charge retention depends on the mechanisms that affect the stored charge quantity and spatial distribution. We assume that electron emission from the nitride to the silicon or the poly-gate is negligible since the bottom and top oxides are thick enough to prevent it. Therefore, the only possible concern is of the lateral charge redistribution in the nitride layer, which results in a threshold voltage variation (ΔV_T) .

Modeling the discharge mechanisms of an NROMTM device is important for better understanding and control of the NROMTM reliability.

In this paper we present a model, which is based on thermally activated electron emission from nitride traps. Tunneling between adjacent sites is neglected. The model allows prediction of the threshold voltage shift as a function of temperature and time for various programming conditions. For example, it predicts a ~ -250 mV threshold voltage shift (ΔV_T) after 10 years at 140°C for an initial 2.5V programming window. It should be noted that this model follows a previous electron emission based model that was developed for MNOS devices.(Lundkvist et al. [4]).

2. The Model

It is assumed that charge loss is due to thermally activated electron emission from nitride traps, where tunneling between adjacent sites is neglected. The electron emission is monitored via threshold voltage (V_T) measurements. The V_T of a programmed cell is given by

$$V_T(t) = V_0 + V_{charge} + \Delta V_T(t) \tag{1}$$

Where V_0 is the threshold voltage of fresh cell, V_{charge} is the change in the threshold voltage due to programming and

 $\Delta V_T(t)$ is the change in threshold voltage due to electron emission.

We define

$$f(t) = \frac{\Delta V_T(t)}{V_{charge}}$$
(2)

Where f(t) is smaller or equal to 1 and was derived experimentally by measuring $\Delta V_T(t)$. The goal of this work is to model f(t) as a function of the traps energy distribution. Doing so will enable predicting $\Delta V_T(t)$ at different temperatures.

The model was established using the following assumptions: 1) The traps are widely distributed over the nitride "bandgap" 2) The emission rates from the distributed traps depend on the energy barrier between the trapped charge and the nitride "conduction band". The emission is thermally activated and its rate follows Boltzman statistics [4]:

$$\tau = \tau_0 \cdot \exp\left(\frac{\phi_\tau}{kT}\right) \tag{3}$$

Where ϕ_{τ} is the trap energy, τ_0 is the reciprocal of the "attempt-to-escape" frequency (~10⁻¹³sec) [5] and T is the absolute temperature. 3) $\Delta V_T(t)$ corresponds to changes in the maximum charge concentration that is located over the n+junction.

4) Most of the traps are empty. Therefore, each emitted electron will be trapped immediately in adjacent sites.

Since according to Eq. (3) the emission time is related to the trap energy, it is convenient to model the function f(t) as $f(\phi_t)$. Thus, $\Delta V_T(t)$ prediction at different temperatures is possible, by interchanging time and temperature. Therefore, the physical meaning of $f(\phi_t)$ is the accumulated energy distribution function of the electron traps. Hence, $\Delta V_T(t)$ corresponds to emission from traps with various energy barriers with different time constants.

3. Experimental details and Results

Samples with the following dimensions were measured: channel width, W=0.35 μ m, effective channel length, L=0.35 μ m, ONO thickness: bottom oxide, T_{bot}=7 nm, nitride, T_{nit}=5 nm and top oxide, T_{top}=9 nm. V_T measurements were taken with low drain-source voltage (V_{DS}=0.1V) to avoid drain induce barrier lowering (DIBL) effect [6]. To evaluate $f(\phi)$, we programmed few cells to $V_{charge}=2.5V$ and than measured $\Delta V_T(t)$ after 20 minutes at different temperatures: 25°C, 90°C, 140°C, 200°C, 225°C, 250°C and 300°C. We also used additional measurement data points after longer times at 300°C to get a better characterization of $f(\phi)$. The derived $f(\phi)$ is presented in Fig. 1. The energy distribution of the electrons traps seems to be spread over the nitride "band-gap" with relatively narrow "peak" charge concentration located at ~ 2.12 eV beneath the "conduction band". In comparison to other works ([4], [7] and [8]) these values are relatively high. For example, in [7] traps depth was found to be 1 eV, in [4] it was found to be widely distributed in the range ~ 1 eV to 2.2 eV, and in [8] it was found to be ~ 0.35 eV and ~ 0.81 eV.

In Fig.1we also added a best-fit function, $f = a \cdot \exp(b \cdot \phi_r)$ (a and b are fitting parameters) which was chosen since it showed good fitting to the data. Note that this approximation is limited to $f < \sim 0.92$. Thus, an interesting result is that more than 90% of the charge that had been stored in traps shallower than 2.3 eV.



Fig. 1. Derived accumulated energy distribution function of electron traps, $f(\phi_t)$.





In Fig. 2, we show a comparison between measurements and calculations of $\Delta V_T(t)$ at temperatures 90°C, 140°C, 200°C and 300°C. Note that the observed and modeled electron discharge span over wide range of temperatures, times and ΔV_T values. For example, after ~ 3 10⁶ seconds, ΔV_T is ~ -190 mV at 140°C where at 300°C it is ~ -2.3V. Based on the model, ΔV_T prediction after 10 years at 140°C is only ~ -250 mV for device programmed to 2.5V. This result indicates that the NROMTM device is a reliable non-volatile semiconductor memory device.

4. Conclusions

A model was developed to describe electron discharge of a localized-charge based novel flash cell. The measured energy distribution of electron traps is relatively high, with maximum concentration located at ~ 2.12 eV beneath the nitride "conduction band". Based on these results, the model fits accurately the experimental results over wide range of time, temperature and $\Delta V_T(t)$ values. Low level of expected $\Delta V_T(t)$ after 10 years in the relevant temperatures implies that the NROMTM technology implies a reliable performance.

References

[1] P. Pavan, R. Bez, P. Olivo, E. Zanoni, "Flash Memory cells - an overview", Proc. of the IEEE, Vol. 85, N.8, pp. 1248-1271, 1997.

[2]Habermehl, R.D. Nasby, M. Rightley, P.R. Mahl, "Endurance of SONOS NVM stacks prepared with Nitrided Si(100)/SiO₂ interfaces," Proc. IEEE NVSMW 98, Monterey, CA, USA, Aug. 2-6, p. 66, 1998.

[3] Boaz Eitan, Paolo Pavan, Ilan Bloom, Efraim Aloni, Aviv Frommer, David Finzi., "NROM: A Novel localized trapping, 2bit non-volatile memory cell ", IEEE Eelctron Dev. Lett, EDL-21 (7), pp.543-545, 2000.

[4] Leif Lundkvist, Christer Svensson and Bertil Hansson, "Discharge of MNOS structures at elevated temperatures", Solid-State Electronics, 1976, vol.19, pp.221-227.

[5] Ingemer Lundstrom and Christer Svensson, "Tunneling to traps in insulators", J. Appl. Phys., Vol. 43, No. 12, December 1972.

[6] Tor A. Fjeldly and Michael Shur, "Threshold Voltage Modeling and the Subthreshold Regime of Operation of Short-Channel MOSFET's ", Transactions On Electron Devices, 40(1), pp.137-145, 1993.

[7] D. F. Bentchkowsky and M. Lenzlinger, "Charge Transport and Storage in Metal-Nitride-Oxide-Silicon (MNOS) Structures, "J. Appl. Phys. 40, No. 8, pp. 3307, 1969.

[8] V. A. Gritsenko, "Excess silicon at the silicon nitride/thermal oxide interface in oxide-nitride-oxide structures", J. Appl. Phys. Vol 86, No. 6, pp. 3234, 1999.