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Time Dependent Anomalous Charge Loss Modeling in Flash Memories and an Accelerated Testing Procedure

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1. Introduction

Data retention is the most critical issue of nonvolatile memories (NVM). Because of the decreasing tunnel oxide thickness, this data retention is determined by a limited population of bits with larger than expected charge loss. This anomalous charge loss has generally been ascribed to the high-field stress during the (tunnel) erase operation. Although several models have been suggested [1-5], up till now there is no commonly accepted charge loss model available. In this paper the direct tunneling model (DT) is proposed to describe the transient behavior of anomalous charge loss, to model accelerated testing by drain disturb, and to derive a simplified analytical method for failure rate prediction.

2. Description of the memory devices and process

The experimental data were obtained on 1Mbit memory circuits based on the HIMOS® approach. This memory cell, which is a Flash-EEPROM device with a split gate structure (Fig. 1), uses Source-Side Injection at the source end of the floating gate channel for programming and Fowler-Nordheim tunneling at the drain for the erase operation [6]. Since programming and erasing occur at different locations, this cell is well-suited for the study of charge loss phenomena associated with the erase operation.

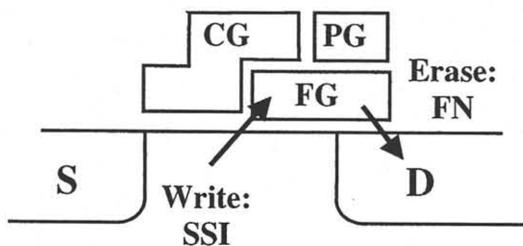

Fig. 1: Schematic view of the HIMOS® cell [6].

The memory circuits were manufactured in a 0.35μm CMOS process with a electrical tunnel oxide thickness of 6.5nm. Because of the dual channel structure with a separate program gate PG, the cell is insensitive to overerase and, therefore, a threshold voltage window with negative as well as positive threshold voltages can be used, as defined from the PG.

3. Theory and modeling

Assuming that anomalous charge loss results from chains of traps in the tunnel oxide and that in each chain only 1 the trap-to-trap step with the largest tunneling distance is limiting the current, the current is described by

$$I_{leak} = \sigma A_{FN} E^2 \exp\left\{ -\frac{4}{3\hbar}\sqrt{2qm^* \phi_t^3}\, \frac{1-\left(1-\frac{Ex_t}{\phi_t}\right)^{3/2}}{E} \right\} \quad (1)$$

where σ is the capture cross section, ϕ_t the trap depth and x_t the trap distance. The time dependence can be described by [7]

$$I_{leak} = c_p \frac{dV_t}{dt} = C_{tot} \frac{dV_{fg}}{dt} \quad (2)$$

where V_t is the threshold voltage and V_{fg} the floating gate (FG) potential. The relationship between V_t and V_{fg} is obtained from a capacitor model which calculates the FG voltage as a function of the external voltages and the FG charge Q_{fg}. Applying the capacitor model to the retention mode and the V_t -measurement mode, respectively, yields two equations. Elimination of Q_{fg} between these two equations gives the following result [8].

$$V_{fg} = V_T + p(V_{pg} - V_t) - s(2\phi_f) + d(V_d - V_{d,read}) + c(V_{cg} - V_{cg,read}) \quad (3)$$

where V_T is the threshold voltage measured at the FG

The electric field is given by $E=(V_d-V_{fg})/t_{ox}$. In case of small fields (retention case) the exponent in equation (1) can be simplified by a Taylor expansion resulting in the approximative analytical solution of differential equation (2):

$$V_t(t) = V_t(t=0s) + V_{t1} \cdot \ln(1 + t/t_1) \quad (4)$$

4. Discussion and applications

4.1 Data retention and failure rate estimation

Fig. 2 shows the experimental data of charge loss at retention conditions (no external voltages) for the erased state as well as the numerical solution of eq. (2) and the approximative solution eq. (4). In Fig. 2a the approximative solution eq. (4) fits the charge loss behavior very well up to the failure level. Although the cell of Fig. 2b has only slightly different parameters, the approximative solution underestimates the failure time. Thus, in any case the approximative solution can be used for a worst case estimation of failure rate.

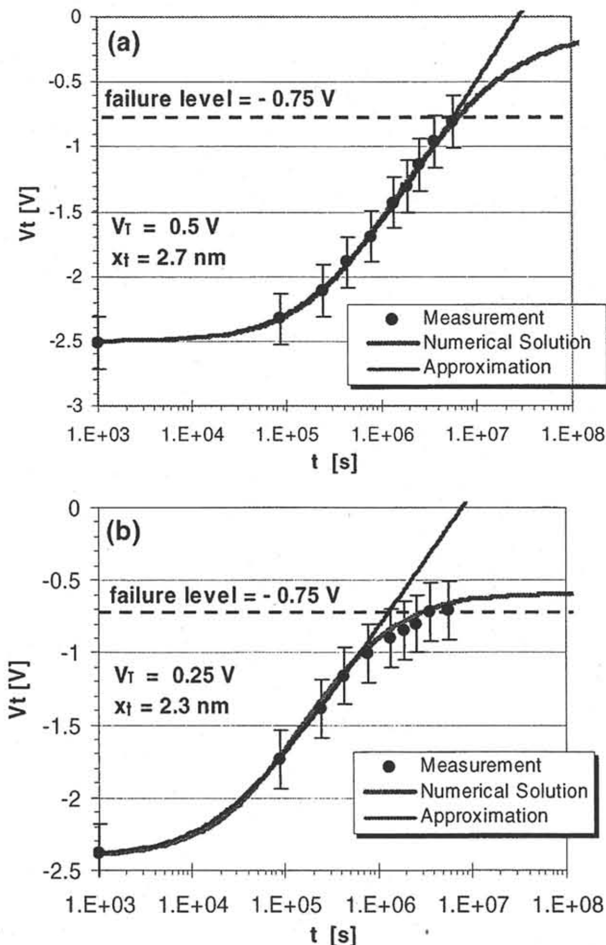

Fig. 2: Measurement (symbols) and simulation (lines) of charge loss of two different cells.

4.2 Test Acceleration

One serious problem of failure rate estimation is the high effort to trace charge loss in commercial products with highly reliable tunnel oxides (oxide thickness around 10 nm) resulting in storage times of up to several months. Though it is possible to accelerate charge loss by external voltages, it was unclear up to now how to extrapolate to retention conditions (without external voltages). As demonstrated in Fig. 3 the numerical solution of eq. (2) can consistently describe charge loss at different drain voltages with one parameter set. Assuming that the conduction mechanism does not change at low fields, these parameters can also be used to calculate the failure time at retention conditions. In this way on can accelerate the failure rate test time and estimate the product's failure rate.

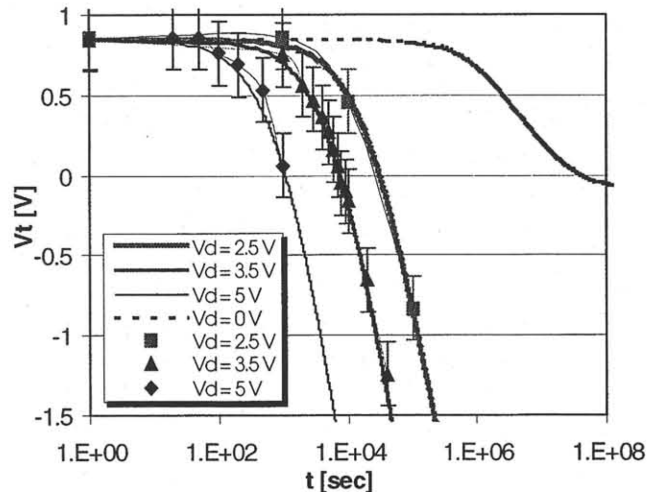

Fig. 3: Experimental data (symbols) of drain disturbs at different drain voltages Vd and their numerical calculation (solid lines) as well as extrapolation to retention condition (Vd=0V, dashed line)

5. Conclusion

It has been shown, that direct tunneling can describe the transient behavior of charge loss. An approximative as well as a numerical solution of the differential equation have been used for estimation of failure times. Since this model scales very well with external voltages, it can also be used to extrapolate disturb measurements to retention conditions.

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