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Bio-Inspired VLSIs Based on Analog/Digital Merged Technologies

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1. Introduction

In the near future, information systems or robots will have flexibility and robustness in recognizing complex objects and understanding real world. Many researches in biology and neuro-science have revealed algorithm of livings and brought out bio-inspired architecture. Last decade, many neural and vision chips were studied by simulating models of the brain and retina. However these trials have provided new techniques, they have not reached to major products. This paper describes new and practical circuit techniques for bio-inspired VLSIs.

2. Features of Bio-inspired System

Bio-inspired systems with a huge number of processing elements operate in massively parallel and analog dynamics. Their operations are very flexible and robust, because they are realized with self-organization and learning mechanism. These principles enable them to realize comprehensive recognition and intuitive judgment based on global information. Furthermore, recent studies in biology have revealed the role of non-linear dynamics and non-deterministic operations. These features are not realized only with the current computer architecture and digital circuits.

3. Merged Analog/digital Circuits using Pulse Signals

Since analog circuits operate based on the physical laws, they have a potential to reduce element counts and power consumption drastically. On the contrary, binary digital signals expressed by discrete time and amplitude, are more accurate comparing with analog one. In order to naturally implement the bio-inspired systems, we have proposed the merged analog/digital circuits using pulse width modulation (PWM) or pulse phase modulation (PPM) signals. [1] While these signals have only two amplitude values, its pulse width/phase represents analog values. The circuit techniques enable the merged use of both analog and digital circuits utilizing extremely scaled and low voltage CMOS devices.

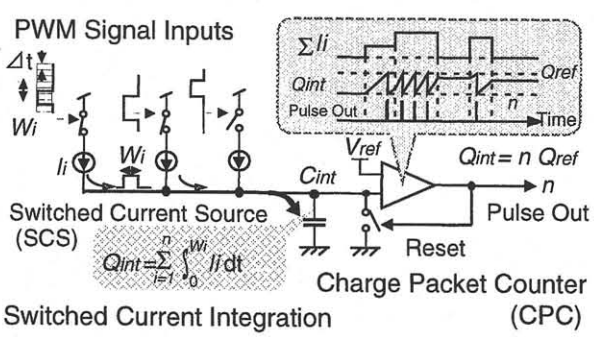

Fig. 1 Linear arithmetic circuit using merged A/D circuit.

4. Linear Arithmetic Circuits using PM signals

We have developed a switched current integration (SCI) and charge packet counting (CPC) techniques that can realize linear arithmetic on the PWM signals as shown in Fig. 1. Utilizing the techniques, multiple input add/sub and multiply and accumulate (MAC) operations can be realized. Operation results given by analog charges are converted to pulse width with a comparator and a linear ramped signal. CPC converts the charge to a binary digital signal.

The linearity error of measured results of 4-input parallel additions and 4-bit multiplication is less than 0.4%, which is determined by the channel length modulation effect of MOS device for current source. A PWM arithmetic circuit dissipates energy E=Ech+Ecmp+Esw in every computation. Ech is charging energy expressed by Vdd Σ IiWi where Ii is i-th current and Wi is i-th pulse width. The comparator energy Ecmp is a dominant component. We compare energy consumption of PWM circuit with that of a digital circuit. Total energy of the A/D merged PWM circuit is around 1/4 of the digital circuit. The advantage is enhanced as the number of inputs increases, because parallel operations are efficiently carried out with lower energy consumption. [2]

5. Image Feature Associative Processor

An Image Feature Associative Processor (IFAP) extracts features of image data, based on bio-inspired PWM architecture has been developed. [3] It consists of a CMOS imager, a cellular automaton (CA), and a pattern matching processor (PMP). Figure 2 shows a block diagram. An experimental chip was designed and fabricated with a 0.8-um CMOS technology as shown in Fig. 2.

Image Sensor: Each pixel generates a PWM pulse with a width proportional to a pixel value for gray-scale readout. The sensor also extracts global features, X/Y projections of binary image for calculating a center of gravity. **Cellular Automaton**: CA

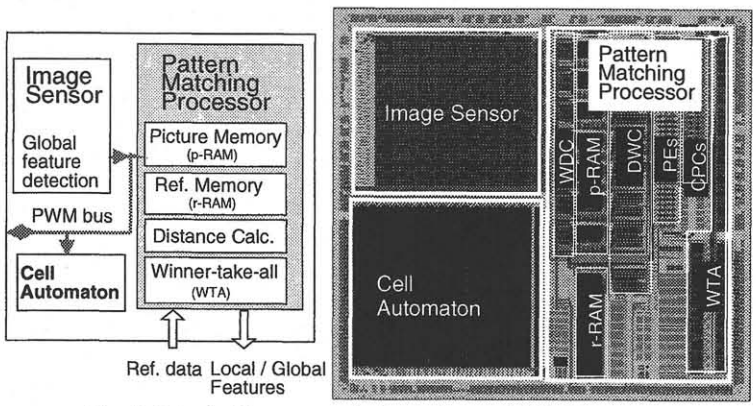

Fig. 2 Block diagram and chip-photo of IFAP.

cell array carries out spatial filter calculations for noise reduction and edge enhancement. Each cell is connected with its 8-nearest neighbor cells with PWM signals and the templates provide the connection strength. **Pattern Matching Processor** (PMP): To extract local features, the most similar reference pattern is associated by the minimum distance search using the PWM arithmetic.[4] A block diagram of PMP is shown in Fig. 3. The Manhattan distance is calculated by the PE, which consists of an EXOR gate for generating PWM absolute difference values as shown in Fig. 4. [5] PMP consumes 120-mW at a 3.3-V power supply. Processing speed per unit power dissipation was 6.75-GOPS/W. The power dissipation of PMP is one-fourth of the simulated value of binary digital circuits.

System application: We have developed a recognition system of hand shape for *Janken*. It implements the algorithm of eye and brain utilizing the IFAP chip for calculating both global and local features. Recognition time was bellow 0.1-sec.

6. Bio-Inspired Nonlinear Systems

We have proposed a nonlinear transform circuit by sampling a nonlinear waveform fN(t) with PWM/PPM signals (Pin) as shown in Fig. 5. [5] The arbitrary NL voltage waveform fN(t) is generated by a look-up table or function generator and D-to-A converter. This means that NL function can be changed in real time and with high controllability. Making feedback loop using the NL circuits, we can implement arbitrary nonlinear discrete-time continuous-state dynamical systems.

Cellular Neural Network (CNN) is a useful model for bio-inspired VLSIs. Utilizing the merged A/D techniques, we have developed the CNN circuit for a multi-functional image processing VLSI.[6] The proposed cell circuit is shown in Fig. 6. Two PWM signals are selected by SEL. DIF calculates the difference of them in a magnitude and a sign bit. The magnitude is transformed by linear/NL function determined fN(t). The PWM output (Pt) updates the cell state (On) based on SCI.

The CNN realizes an image segmentation based on a resistive-fuse network model. An iterative operation of each CNN circuit obtains the minimum energy state by a steepest descent method as shown in Fig. 7. A Gabol filter for local feature detection is also realized with the same CNN. We can also implement a chaos generator using PM Signals. This can realize stochastic processing as a random number generator. [7]

7. Conclusion

The merged analog/digital circuits utilizing pulse modulation signals have been proposed. They can implement the multi-input linear arithmetics and the discrete-time nonlinear dynamics for bio-inspired VLSIs with human-like intelligence.

References

[1] A. Iwata, et al., IEICE Trans. A, E-79-A, 145-157 (1996)
[2] M. Nagata, et al., IEEE JSC, 33, 53-60 (1998)
[3] A. Iwata, et al., IFAP Int. Conf. VLSI, 77-88 (1999)
[4] H. Nakamoto et al., SSDM1999, 998-99 (2000)
[5] T. Morie, et al., NOLTA'98, 449-450 (1998)
[6] T. Morie, et al., ICONIP2000, 613-617 (2000)
[7] K. Murakoshi, et al., ASP-DAC2000, 100-101 (2000)

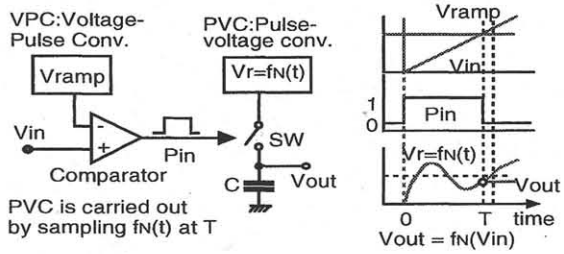

Fig. 5 Nonlinear transform circuit using PM Signals

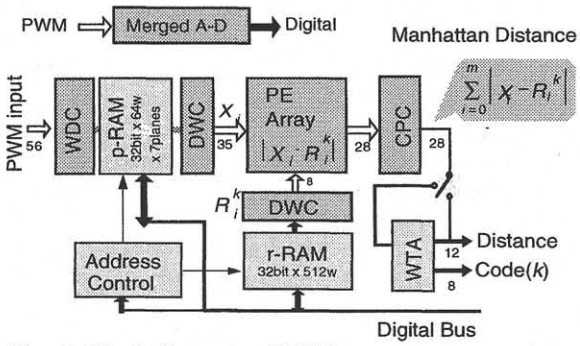

Fig. 3 Block diagram of PMP.

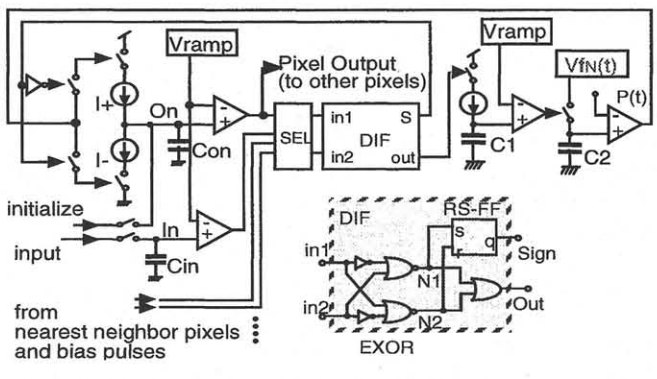

Fig. 6 CNN cell circuit using PWM signals

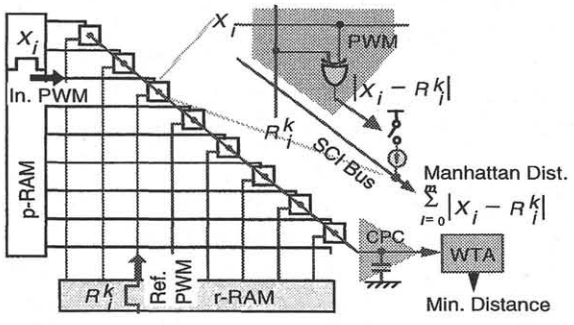

Fig. 4 Manhattan distance calc. using PWM Signals

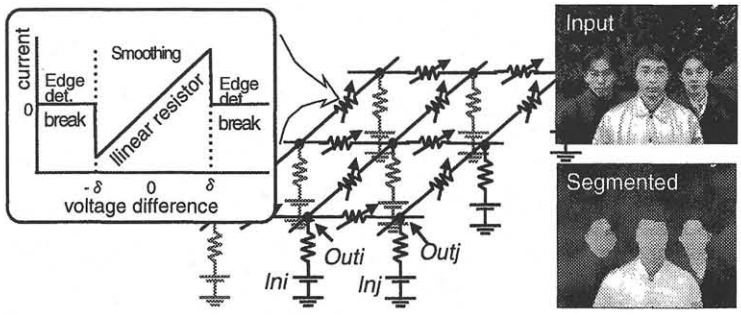

Fig. 7 Resistive fuse network for image segmentation