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A High-Performance Time-Domain Winner-Take-All Circuit Employing OR-Tree Architecture

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1. Introduction

Vector quantization (VQ) [1] plays an essential role in a number of signal processing systems like associative memories, Kohonen's self-organizing maps, audio/visual data compression systems, image recognition systems and so forth. In vector quantization, the distance between an input vector and each template vector is computed in the first place, and then the template vector having the minimum distance to the input vector is identified as the winner. In hardware implementation of VQ systems, the circuit carrying out the winner search in a large number of template vectors is called winner-take-all (WTA). High-speed search for the winner is a primary concern of the WTA.

The first WTA circuit was developed using a current-mode technique in the MOS subthreshold regime [2], and several other current-mode circuits [3] have been reported. The WTA in a voltage mode of operation was first developed using the vMOS technology [4] as shown in Fig. 1. The circuit is composed of multiple chopper comparators having two equally-weighted vMOS inputs where V_0~V_n are voltage inputs representing distances calculated by vMOS analog vector matching circuits. The magnitude of the voltage is converted to a delay time using a common ramp-up signal (V_{ramp}). The winner is detected as the first upsetting comparator. The first upsetting signal is fed back to each comparator through a multiple-input OR to close the latch switch, thus freezing its output state at the moment of the winner upsetting. The problem of this circuit is that several other comparators have chance to upset before the OR output signal arrives due to the finite delay in the OR circuitry.

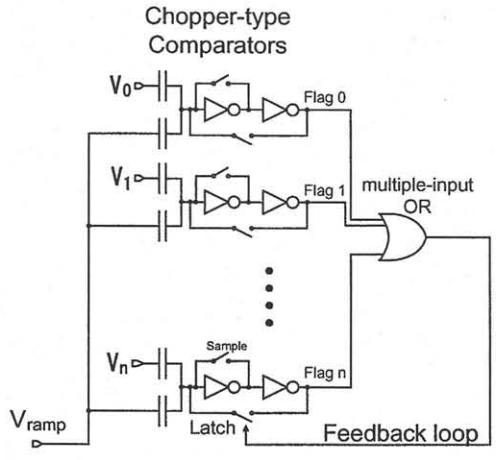

Fig. 1. vMOS WTA circuit employing a feedback loop via multiple-input OR [4].

The RS flip-flop tree architecture was introduced in Ref. [5] to detect the first arrival of a non-zero pulse, where the Hamming distance between two binary codes was converted to the delay of a propagating pulse.

The purpose of this paper is to develop a high performance WTA using the ramp-voltage technique for distance-to-delay conversion and the tree architecture for delay detection. However, a simple OR-tree was employed instead of the RS flip-flop tree in Ref. [5] to enhance the speed and accuracy. As a result, 8-bit accuracy search for 64 distance inputs has been experimentally demonstrated at a ramp rate of 5V/250~350nsec.

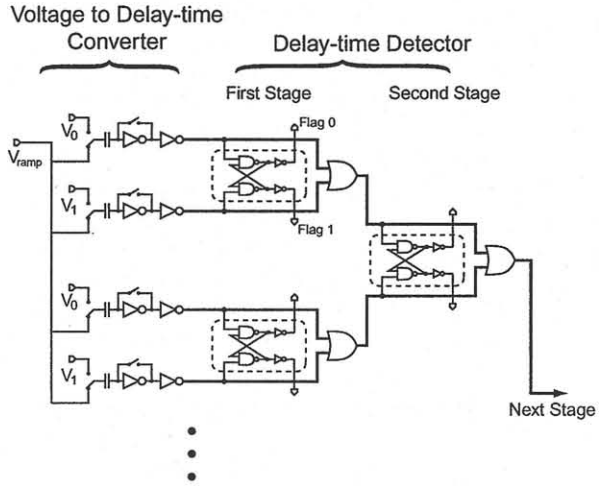

Fig. 2. WTA circuit employing open-loop OR-tree architecture.

2. OR-tree Winner-Take-All Circuit

The WTA circuit developed in this work is showed in Fig. 2. The circuit consists of two parts: a voltage-to-time converter where the vMOS inputs were replaced by a single-capacitor input as compare to the one in Fig. 1; a delay-time detection circuit.

The delay-time detector is built in a simple OR-tree architecture. At each input stage of an OR circuit, a flip-flop latch is attached in parallel to the OR. The flip-flop detects which node upsets first, and stores the result. In other words, the winner position is memorized in the open-loop configuration. As a result, there is no problem of time delay in the feedback loop.

In the time-domain WTA in Ref. [5], the output of the flip-flop is directly connected to the next flip-flop input. The problem is that it takes a long time for the flip-flop to settle in a stable state when two input signals arrive at almost the same time. This delays the winner signal to propagate to the next stage, leading to an error in the winner detection. However, this dose not occur in the OR-tree circuitry.

In this work, a latching comparator and a dynamic logic gate were employed for the flip-flop and the OR, respectively as illustrated in Fig. 3. The sink current in the OR is limited by a proper sizing of the bottom NMOS, thus further reducing the variation in the logic set-up time depending on whether the input is "0, 1" or "1, 1".

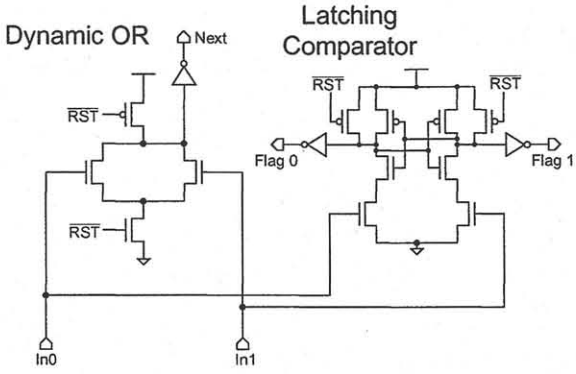

Fig. 3. Latching comparator attached in parallel to the OR tree.

3. Results and Discussion

A test WTA circuit having 64 inputs was designed and fabricated in a 0.6-μm CMOS technology. A photomicrograph of the test chip is given in Fig. 4, and an example of test chip measurements is demonstrated in Fig. 5.

The performance of the WTA circuit using the OR-tree architecture and that of the WTA circuit using a 64-input domino-logic OR in a feedback loop (as shown in Fig. 1) were compared by the post-layout HSPICE simulation. In order to achieve an 8-bit resolution accuracy in the latter, the ramp-up time greater than 1.5μsec is required for the voltage swing of 5V. While, the ramp-up time as short as 160nsec is sufficient in the former

In the test circuit, the ramp-up voltage was internally generated using a pMOS current source. From the measurement results, it was found that the OR-tree achieves the time resolution of 500~700psec and that the voltage resolution of 8 bits is obtained at a ramp-up rate of 5V/250~350nsec.

4. Conclusion

A high-performance WTA circuit has been developed employing an open-loop OR-tree architecture. The WTA circuit can operate about ten times faster than the conventional WTA circuit employing feedback loop via multiple-input OR.

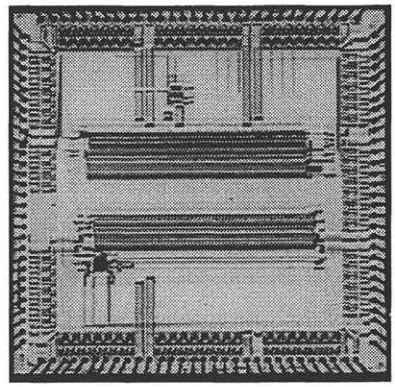

Fig. 4. Photomicrograph of the test chip.

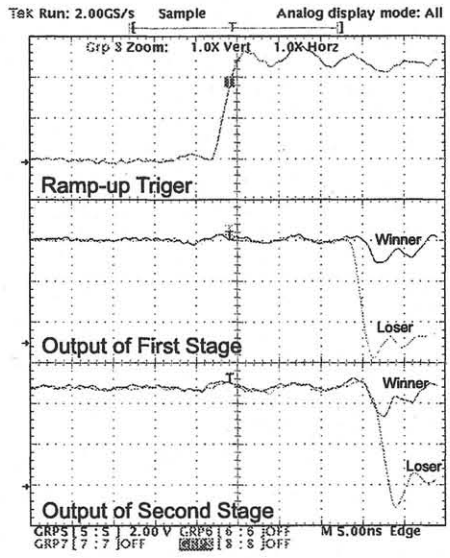

Fig. 5. Measured waveforms of a test circuit.

Acknowledgments

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

References

[1] A. Gersho and R. M. Gray, *Vector Quantization and Signal Compression*. Boston, MA: Kluwer Academic, 1992.

[2] J.Lazzaro, R. Ryckebusch, M. A. Mahowald, and C. Mead, "Winner-take-all networks of O(n) complexity," in *Advances in Neural Information Processing Systems 1*, D. S. Touretzky, Ed. Los Altos, CA: Morgan Kaufmann Publishers, 1989, pp. 703 – 711.

[3] G Cauwenberghs and V. Pedroni, "A Charge-Based CMOS Parallel Analog Vector Quantizer," in *Advance in Neural Information Processing Systems 7*, eds G Tesauro, D. S. Touretzky, and T. K. Leen, MIT Press, Cambrigde MA, 1995, pp. 779-786.

[4] T. Yamashita, T. Shibata and T. Ohmi, "Neuron MOS winner-take-all circuit and its applicaton to associative memory," em ISSCC Dig. Techinical papers, FA 15.2, Feb, 1993, pp. 236 – 237.

[5] M. Ikeda and K. Asada, "Time-domain Minimum-Distance Detector and Its Application to Low Power Coding Scheme on Chip Interface," 24th European Solid-State circuit Conference(ESSCIRC), 1998, pp. 464-467.