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$Si_{1-x}f120Ge_x$/Si Triple-Barrier RTD with a Peak-to-Valley Ratio of ≥ 180 at RT Formed Using an Annealed Thin Multilayer Buffer

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1. Introduction

Resonant-tunneling-diode (RTD) quantum devices have attracted considerable attention as promising devices for future ultrahigh-speed and low-dissipation applications. In addition to these merits, SiGe RTDs have also been focused for their potential feasibility of being integrated with Si CMOS circuits [1]. However, only RTDs made from III-V materials have been applied in practice to logic circuits because of their much larger negative-differential-resistance (NDR) resonances than those of SiGe RTDs. The degree of the NDR effect is determined using the peak-to-valley current ratio (PVR) as a figure of merit, and for III-V RTDs, PVR values of more than 50 are obtained at room temperature (RT) [2]. For quantum devices to be useful, they must operate at RT [1].

As for SiGe RTDs, RTD structures have been designed mainly for hole tunneling, since large valence band offsets are easily obtained. A double-barrier (DB) and a triple-barrier (TB) structure have been applied to these RTDs; however, they exhibit poor temperature performance with a PVR value of approximately 2 at temperatures of ≤ 77 K and the NDR has not been observed at RT due to thermally assisted tunneling through closely spaced light-hole and heavy-hole levels [3]. On the other hand, Ismail *et al.* observed for the first time an electron-tunneling NDR at RT [4]. All reported electron-tunneling RTDs have a double-barrier (DB) structure and the highest PVR value has been 2, which was measured at 4.2 K [5]. On the basis of our theoretical analysis, we have recently applied for the first time a combination of electron tunneling with a single mass and multiple wells to a SiGe RTD, and have demonstrated that an electron-tunneling $Si_{0.7}Ge_{0.3}$/Si triple-barrier (TB) RTD exhibits a PVR value of ≥ 7.6 at RT [6] which is ~ 4 times as high as the previously reported highest value of 2 measured at 4.2 K [5].

In this paper, to further improve the NDR characteristics, we optimize the layer structure and growth method for the TB RTD and propose the use of an annealed thin stepwise $Si_{1-x}Ge_x$ multilayer as a strain-relief relaxed buffer on which the TB structure is grown. As a result, an electron-tunneling $Si_{0.67}Ge_{0.33}$/Si TB RTD formed using the annealed thin double-layer buffer exhibits a PVR value of ≥ 180 at RT which is comparable to the values obtained from III-V RTDs.

2. Experimental

Si and $Si_{1-x}Ge_x$ layers were grown on 0.8-1.2 Ω-cm n-type Si(001) substrates using a gas-source molecular-beam epitaxy (MBE) techniques with GeH_4 and Si_2H_6. All layers were grown under a substrate temperature of 600 °C. For electron tunneling, the type II band configuration is used and a well is created using the structure of tensile-strained Si well sandwiched between unstrained $Si_{1-x}Ge_x$ barriers. To obtain the unstrained $Si_{1-x}Ge_x$ layer, a strain-relief relaxed buffer is formed on a Si(001) substrate. When $x > 0.3$, a barrier height of >0.18 eV is obtained according to the calculation using the deformation potential model [6, 7]. In this work, we have studied of the formation of a strain-relief relaxed $Si_{1-x}Ge_x$ buffer with a high crystalline quality surface where $x > 0.3$.

3. Results and Discussion

First, we investigated the relationship between the lattice spacing and the growth thickness for a single $Si_{0.79}Ge_{0.21}$ layer grown on Si(001), and the anneal effects on the lattice spacing and the relaxation. The results are shown in Fig. 1. Single $Si_{0.79}Ge_{0.21}$ layers of 7300 and 3700 Å thicknesses are relaxed by 75 and 66 %, respectively. The postanneal causes further lattice relaxation. In Fig. 2, the lattice spacing, relaxation degree and surface crystalline quality are compared between single $Si_{0.79}Ge_{0.21}$ (#1) and $Si_{0.67}Ge_{0.33}$ (#2) layers, and $Si_{0.67}Ge_{0.33}$-on-$Si_{0.79}Ge_{0.21}$ double layers (#3 - #7). These layers were grown on Si(001). The data were taken for as-grown samples (#1-#6) and after a postanneal at 700 °C for 10 min (#7). A single $Si_{0.67}Ge_{0.33}$ layer of 1200 Å thickness (#2), the thickness of which is larger than the $Si_{0.67}Ge_{0.33}$ critical thickness of misfit dislocation generation (~ 400 Å) [8] exhibits 89 % relaxed surface; however, the surface has very poor crystalline quality as shown in Fig. 2. On the other hand, using a 1200-Å-$Si_{0.67}Ge_{0.33}$-on-3700-Å-$Si_{0.79}Ge_{0.21}$ double layer (#3), the top layer is relaxed by 94 % and the crystalline quality of the top surface is considerably improved; however, there are still many dislocation defects observable in the SEM image. When the top layer thickness is reduced to 600 Å (600-Å-$Si_{0.67}Ge_{0.33}$-on-3700-Å-$Si_{0.79}Ge_{0.21}$ (#5)), the crystalline quality of the top surface (relaxed by 89 %) is improved; however, many defects are still observed. When the lower layer thickness is reduced to 1200 Å (1200-Å-$Si_{0.67}Ge_{0.33}$-on-1200-Å-$Si_{0.79}Ge_{0.21}$ (#4)), the number of the top surface defects becomes larger than that of the #3 sample. The increase is explained by the increase in the lattice mismatch from 0.8 to 1.2 % between the two growth layers. When the thicknesses of both the layers are reduced (600-Å-$Si_{0.67}Ge_{0.33}$-on-1200-Å-$Si_{0.79}Ge_{0.21}$ (#6)) , the surface quality is much considerably improved with little defects; however, the top surface relaxation rate decreases to 74 %. However, by annealing the #6 sample, highly-relaxed $Si_{0.67}Ge_{0.33}$ (> 89 %) surface having

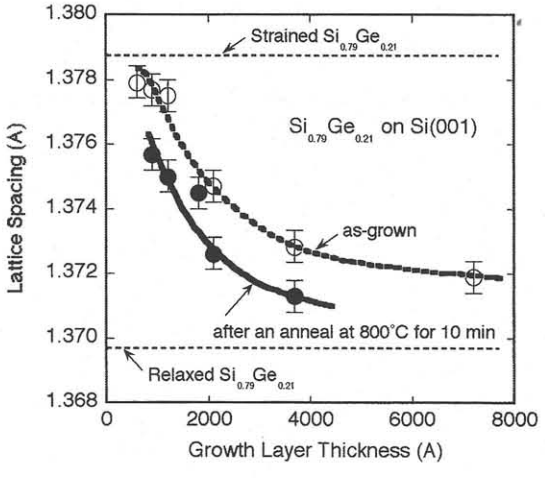

Fig. 1 Lattice spacings obtained from as-grown $Si_{0.79}Ge_{0.21}$ layers grown on Si(001) and after annealing $Si_{0.79}Ge_{0.21}$ layers grown on Si(001).

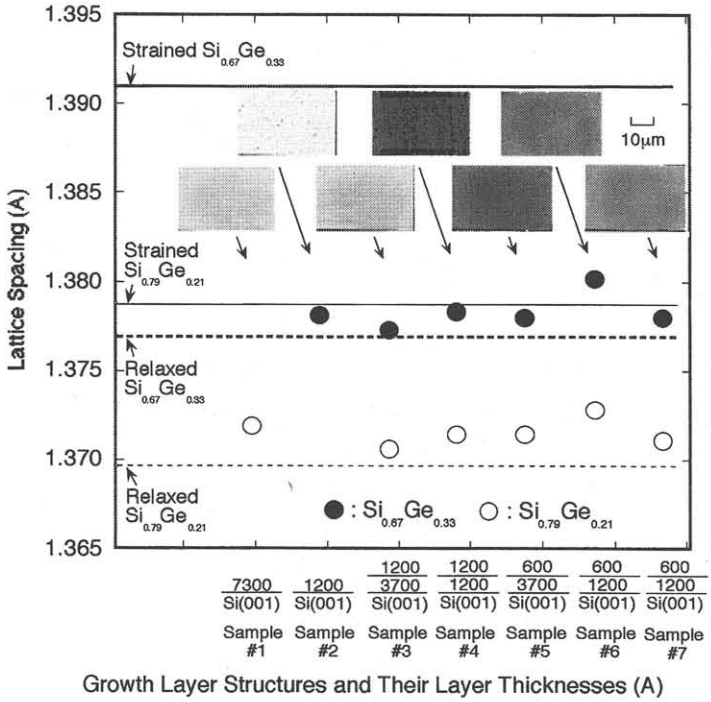

Fig. 2 The lattice spacing (relaxation degree) and surface crystalline quality (SEM image) are compared between single $Si_{0.79}Ge_{0.21}$ (#1) and $Si_{0.67}Ge_{0.33}$(#2) layers, and $Si_{0.67}Ge_{0.33}$-on-$Si_{0.79}Ge_{0.21}$ double layers (#3 - #7). These layers were grown on Si(001). The data were taken for the as-grown samples (#1-#6) and after a postanneal at 700 °C for 10 min (#7).

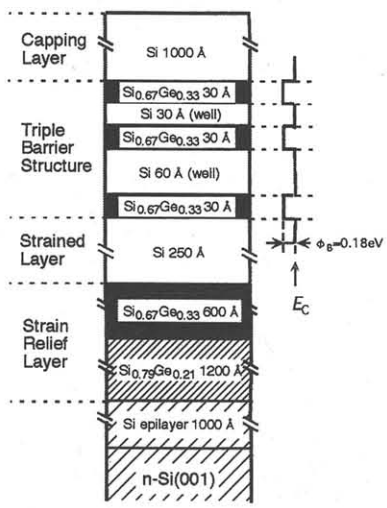

Fig. 3 Structure of a $Si_{0.67}Ge_{0.33}$/Si asymmetric triple-barrier (TB) RTD and the band lineup calculated using the model of Van de Walle and Martin [7].

high crystalline quality with little defects was obtained as shown in Fig. 2.

We have applied the annealed thin 600-Å-$Si_{0.67}Ge_{0.33}$-on-1200-Å- $Si_{0.79}Ge_{0.21}$ double-layer buffer with high surface crystalline quality to electron-tunneling $Si_{0.67}Ge_{0.33}$/Si TB RTD. For this RTD, we designed the asymmetric TB structure to cause the resonance tunneling effectively on the basis of the theoretical *I-V* curve calculation. The structure of this RTD is shown in Fig. 3 and the experimentally obtained *I-V* curve measured at RT is shown in Fig. 4. The PVR value is as high as > 180 which is ~ 100 times as high as those reported by other researchers and comparable to those obtained from III-V RTDs.

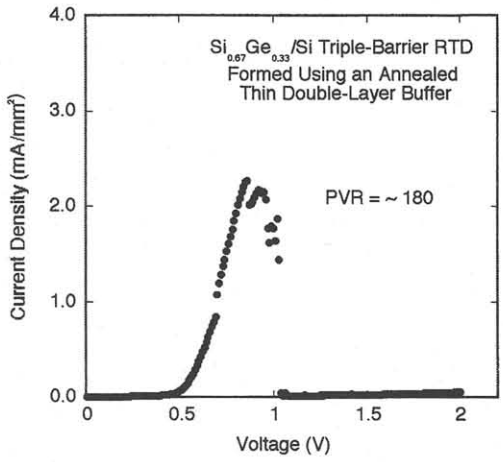

Fig. 4 A typical *I-V* curve obtained at room temperature from a $Si_{0.67}Ge_{0.33}$/Si asymmetric triple-barrier RTD formed using the annealed thin double-layer buffer. The data shows a PVR value as high as ~ 180 which is comparable to the values obtained from III-V RTDs.

4. Conclusions

we have further optimized the layer structure and growth method for our previously proposed electron-tunneling $Si_{1-x}Ge_x$ TB RTD device and have proposed the use of an annealed thin stepwise $Si_{1-x}Ge_x$ multilayer as a strain-relief relaxed buffer on which the TB structure is grown. By annealing a thin 600-Å $Si_{0.67}Ge_{0.33}$ / 1200-Å $Si_{0.79}Ge_{0.21}$ double layer, we have obtained a strain-relief $Si_{0.67}Ge_{0.33}$ buffer which is relaxed by 89 % and has a surface with high crystalline quality. An electron-tunneling asymmetric $Si_{0.67}Ge_{0.33}$/Si TB RTD formed using this buffer exhibits a low background current and a PVR value of ≥ 180 at RT which is ~ 100 times as high as those reported by other researchers and is comparable to the values of III-V RTDs. The high PVR behavior is explained as being related to the strain-relief relaxed buffer surface with high crystalline quality and low dislocation and defect density. The proposed RTD layer structure and growth method give rise to great potential to SiGe RTDs for future practical integrated device applications.

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