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Resonant Tunneling Effect in Si/SiO_2 Double Barrier Structure

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1. Introduction

Up to now, in Si/SiO_2 systems, clear observation of negative differential resistance (NDR) due to resonant tunneling effect has not been reported, although a few non-linear *I-V* curves were ascribed to the resonant tunneling effects [1,2]. This is probably because it is difficult to fabricate SiO_2/single-crystalline-Si/SiO_2 sandwich structures in contrast to hetero-epitaxy systems such as GaAs/AlGaAs structures.

In this work, in order to clarify the presence of the resonant tunneling effect in Si/SiO_2 system, *I-V* measurements were performed for SiO_2/single-crystalline-Si double barrier diodes. The diodes were fabricated from a silicon-on-insulator (SOI) wafer having an ultrathin (~2 nm) buried SiO_2 (BOX) layer, which was developed by the authors [3]. As a result, we observed, for the first time, a clear NDR with the peak-to-valley ratio (PVR) of ~1.8, indicating the resonant tunneling effect in ultrathin SiO_2/Si structure.

2. Fabrication of SiO_2/Si Double Barrier Diodes

Instead of conventional deposition techniques, which cannot form single-crystalline Si layer on SiO_2, the following process was applied to the sample preparation, where a special SOI wafer was used as the starting substrate.

The starting SOI wafer is schematically shown in Fig. 1(a). The most important point is that this wafer has an ultrathin (~2 nm) thermally grown BOX layer, which permits electron tunneling between the top Si layer and the n^+ base substrate. (In the final structure, this BOX layer works as a lower barrier layer.)

Since such an SOI wafer with the ultrathin BOX is not commercially available, the wafer was fabricated in our laboratory by a wafer bonding technique, whose details have been described elsewhere [3]. In the bonding process, (001) wafers were used for both of the top Si and the base substrates. Additionally, in-plane direction of the top Si layer was carefully aligned to be parallel to that of the base substrate.

Ultrathin double barrier structure is obtained after the thinning of the top Si layer to nanometer range (by oxidation and the oxide removal) and after the oxidation for the formation of an upper barrier layer (~2-nm-thick SiO_2). It is noted that the structure is composed of single-crystalline Si and thermal SiO_2. In fact, TEM images in Fig. 2 reveal the ultrathin (~2 nm ± 0.3 nm-rms) single-crystalline-Si layer sandwiched between SiO_2 layers.

For the *I-V* characterization, local oxidation was made for 10-μm-scale patterning of the Si layer (isolation of the neighboring diodes). The resultant structure is schematically shown in Fig. 1(b). As the top electrodes, Al was deposited by the conventional vacuum evaporation. The interface state density was reduced by annealing the sample in H_2/N_2 mixture.

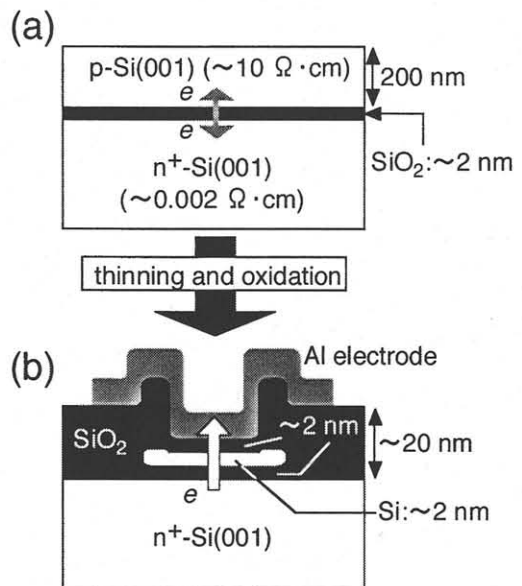

Fig. 1. Schematic illustrations of (a) SOI wafer with an ultrathin BOX layer and (b) fabricated SiO_2/single-crystalline-Si double barrier diode.

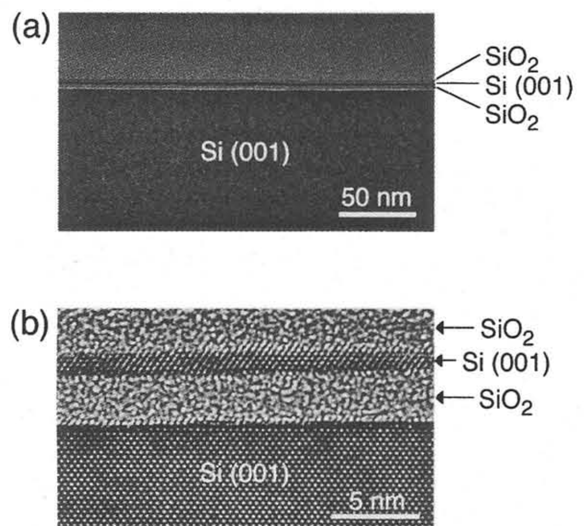

Fig. 2. Typical TEM images for fabricated SiO_2/single-crystalline-Si double barrier structure.

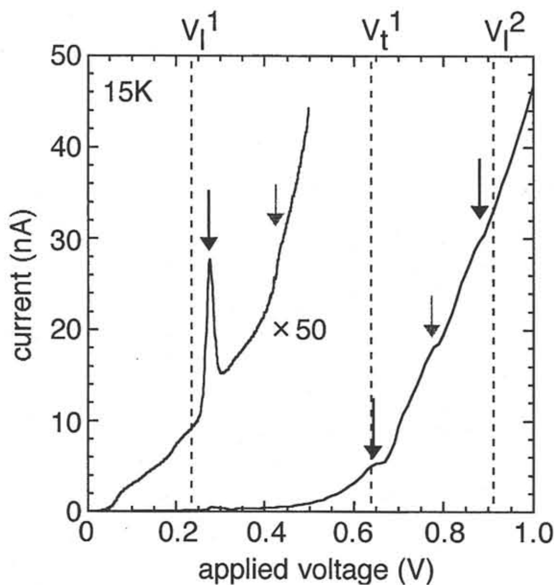

Fig. 3. Typical *I-V* curve for a diode with the Si thickness of ~2 nm.

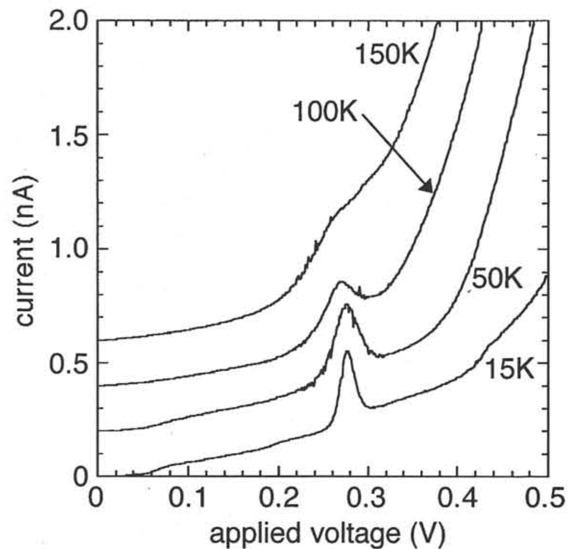

Fig. 4. Temperature dependence of *I-V* curve for a diode with the Si thickness of ~2 nm.

3. *I-V* Characteristics and Discussion

Figure 3 shows a typical *I-V* curve for a diode with the Si thickness of ~2 nm (15K, diode area: ~150 μm^2). Here, positive voltage was applied to the Al electrode, corresponding to electron transport from the n^+-Si substrate to the Al electrode.

A clear NDR with the PVR of ~1.8 was repodicibly observed at V = 0.28 V, together with inflections of the *I-V* curve indicated by the arrows. To our knowledge, this is the first observation of NDR in Si/SiO_2 system. This NDR feature was observed up to ~150K, as shown in Fig. 4.

In order to examine whether the observed NDR is ascribed to the resonant tunneling effect, resonance voltages were theoretically calculated, taking into account the anisotropy of electron mass for Si (001) plane ($m_l = 0.98m_0$ and $m_t = 0.19m_0$). Dashed lines in Fig. 3 represent the resonance voltages for the Si thickness of 1.6 nm. (V_l^i is for m_l, while V_t^i is for m_t (i: level index).) These values are found to almost agree with the ones for the NDR and the inflections, although some inflections do not fit, probably due to other effects such as phonon emission. Thus, it is concluded that the observed NDR is due to the resonant tunneling of electrons through the ultrathin Si layer.

4. Conclusion

SiO_2/single-crystalline-Si double barrier diode was fabricated from a bonded SOI wafer with an ultrathin BOX layer. We observed, for the first time, a clear NDR (PVR of ~1.8) in the *I-V* curve, which is ascribed to the resonant tunneling effect.

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References

[1]K. Yuki, Y. Hirai, K. Morimoto, K. Inoue, M. Niwa and J. Yasui, Jpn. J. Appl. Phys. **34** (1995) 860.
[2]H. Namatsu, S. Horiguchi, Y. Takahashi, M. Nagase and K. Kurihara, Jpn. J. Appl. Phys. **36** (1997) 3669.
[3]Y. Ishikawa, M. Makita, J. Zhang, T. Tsuchiya and M. Tabe, Jpn. J. Appl. Phys. **38** (1999) L789.