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Fluoride Resonant Tunneling Diodes Co-Integrated with Si-MOSFETs

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1. Introduction

Heteroepitaxial structures composed of CaF_2 and CdF_2 grown on Si substrates are interesting in that it may be possible to use such structures to introduce quantum-effect devices into Si integrated circuits. The favorable conditions in the particular material system are that the lattice mismatch of CaF_2 and CdF_2 to Si at room temperature is +0.6% and -0.8%, respectively, and the electron affinity of CdF_2 is as large as that of Si while that of CaF_2 is very small. Thus, deep quantum well structures of $CaF_2/CdF_2/CaF_2$ can be grown on Si directly. Resonant tunneling diodes (RTDs) operating at room temperature have already been reported [1,2], and extremely large peak to valley current ratio (P/V ratio) was reported recently [2].

It is known that various digital circuits composed of RTDs and FETs can be formed with smaller number of devices comparing to the conventional circuits of equivalent function using FET only [3]. This is attractive for Si integrate circuit since it can contribute in enhancing high-integration effectively.

Previous investigation on RTDs composed of fluoride heterostructures were for discrete devices simply formed on a flat n-type Si substrate and observation of I-V characteristics of the independent devices. In this paper, we present a process developed to fabricate fluoride RTD on heavily doped ion implanted region, and fabrication of a test circuit in which fluoride RTDs and a conventinal n-MOSFET were co-integrated on a Si substrate.

2. RTD formed on heavily ion-implanted region

In order to realize the co-integration, it is necessary that the ultra thin fluoride heterolayers are grown on n^+ region on a Si surface which are usually formed by ion implantation with high dose. However, if deterioration of flatness of the Si surface in atomic layer level occurred, the RTD properties may be affected by the roughness of the substrate since each layer of the fluoride is very thin. Thus, we have investigated the effects through fabrication of the fluoride RTDs as shown in Fig.1.

First, an n-type Si(111) wafer was thermally oxidized , and contact holes were opened. Then, 100keV P^+ ions were implanted to the bottom of the hole with various dose. After chemical cleaning process, the as implanted substrate was loaded in the MBE growth chamber. The sample was heated at 850°C in the UHV for both thermal flashing to obtain clean Si surface and activation of implanted ions. Next, $CaF_2/CdF_2/CaF_2$ layers were grown on the sample, where thickness and growth temperature for each layer are those indicated in the Fig.1. Finally, Al was evaporated on both sides of the sample and top electrodes were formed by wet etching.

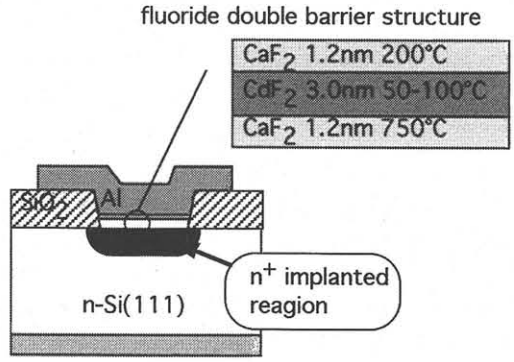

Fig.1 Strucutre and growth conditions of fluoride RTD.

On the way of the process described above, some samples finished in the annealing in UHV and before the fluoride growth were taken out of the chamber and their Si surfaces were observed by atomic force microscopy (AFM). Figure 2 shows surface roughness vs ion dose. It was found that surface roughness was reduced to close to non-implanted case for dose less than $3x10^{15}cm^{-2}$, but it was drastically increased for dose of $1x10^{16}cm^{-2}$. RTDs were fabricated on such surfaces and their I-V characteristics were observed. RTDs for ion dose less than $3x10^{15}cm^{-2}$ exhibited good characteristics with rather high yield, but the yield of RTDs for ion dose of $1x10^{16}cm^{-2}$ was very low. This result is consistent with the increase of the surface roughness as shown in Fig.2.

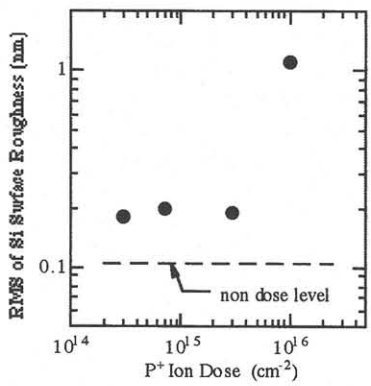

Fig.2 Roughness of ion implanted Si surface vs ion dose.

3. Fabrication of circuit composed of fluoride RTD and Si n-MOSFET

As a test circuit to show feasibility of the co-integration, the circuit composed of two fluoride RTDs and one n-MOSFET as shown in Fig.3 was fabricated. This circuit is known to have a function of 1-bit SRAM cell. Operation of this circuit using Si interband tunneling diodes has been reported recently[4]. The cross section diagram of a RTD and MOSFET connected in series is shown in Fig.4. Fabrication process was similar to that described in section 2, in which RTD and MOSFET were formed simultaneously. P^+ ion dose was chosen to be $3x10^{15}cm^{-2}$, considering the surface roughness as discussed in section 2 and ohmic contact properties of Al and Si. An optical micrograph of the circuit fabricated is shown in Fig.5. The size of the FET was W/L=75μm/5μm and the area of RTD was 10μm x 10μm.

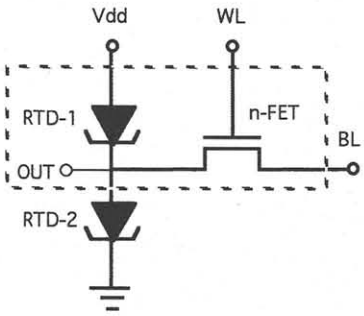

Fig.3 Circuit composed of RTDs and n-MOSFET.

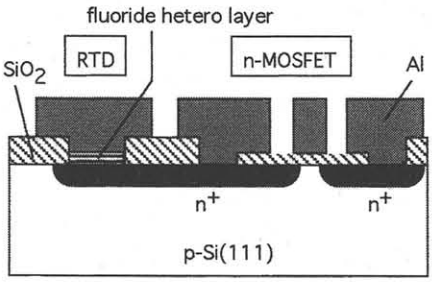

Fig.4 Cross section of integrated RTD and n-MOSFET.

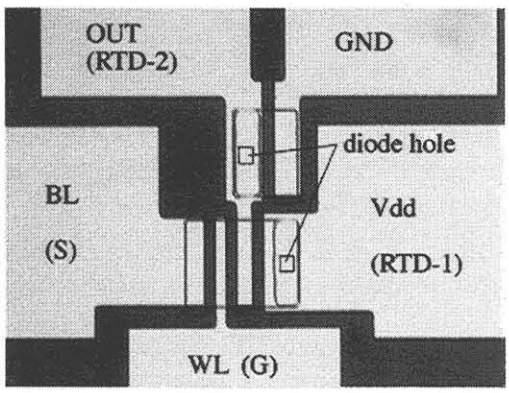

Fig.5 Optical micrograph of a fabricated circuit.

I-V characteristics of the RTDs were observed independently, and an example is shown in Fig.6. P/V ratio of 25 was obtained at room temperature. It was shown that the fabrication process used here worked well to form the RTDs.

Figure 7 shows V_{out} vs V_{dd} characteristics for the two series RTDs. The hysteresis characteristics was observed and bistabe operation of the integrated circuit was confirmed.

SRAM operation using all component in this circuit is now under investigation.

4. Conclusion

Co-integration of fluoride ($Al/CaF_2/CdF_2/CaF_2/Si$ double barrier) RTDs and Si n-MOSFETs for application to integrated circuits has been realized for the first time. The RTD characteristics (P/V ratio: 25) comparable to those in the previous works was obtained in spite of the using high dose ion implantation process. Bistable operation of the integrated two RTDs structure was observed.

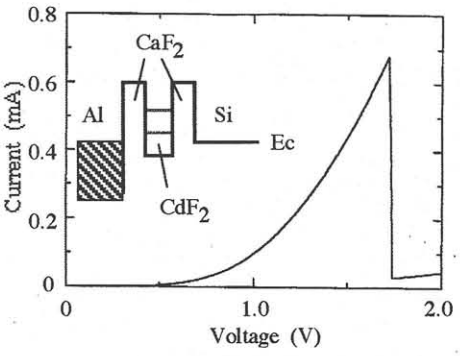

Fig.6 I-V characteristics of one RTD in the fabricated circuit. Inset represents band alignment of the RTD.

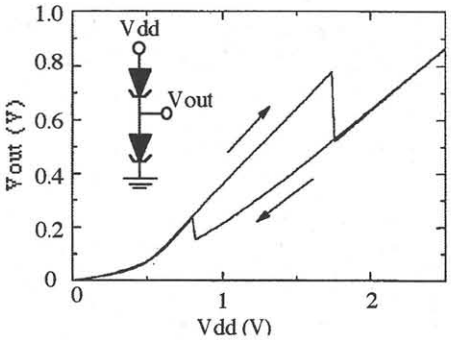

Fig.7 Vout vs Vdd characteristics for two RTDs series connection in the circuit.

References

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