Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 98–99

D-2-1 (Invited)

Low Power Technologies for High Performance Systems

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Introduction

CMOS power dissipation has been increasing due to the increase in power density as shown in Fig. 1. The power dissipation increased fourfold every three years until the early 1990's, due to a constant voltage scaling. Recently, a constant field scaling has been applied to reduce power dissipation, where the power density is increased proportional to the 0.7^{th} power of scaling factor, leading to power increase by twice every 6.5 years. It is considered that the power dissipation of CMOS chips will steadily be increased as a natural result of device scaling, approaching to an upper limit in terms of chip heat limit.

When the industry was prompted to shift from bipolar and NMOS technologies to CMOS technology in the mid-80's in order to alleviate heat removal problem, CMOS was on the horizon. However, the supplanting of CMOS by yet another more energy efficient technology remains a distant prospect now. Hence, a low-power, high-performance CMOS technology is an indispensable technology. In this paper, recent research results are reviewed, especially in circuit design, and the impact to CMOS life span is discussed.

Lowering Supply Voltage

In order to maintain chip performance at low supply voltages (V_{DD}'s), there are three approaches: (a) utilize parallel and/or pipeline architectures to compensate for the degraded circuit speed, (b) lower threshold voltage (V_{TH}) to recover the circuit speed, and (c) lower V_{DD} only for non-critical circuits. In the second approach V_{DD} and V_{TH} should be optimized according to speed requirement from time to time (hence, variable), while in the third approach they should be optimized spatially from circuits to circuits (hence, multiple).

A Variable Threshold-voltage CMOS technology (VTCMOS) [1] is developed to control V_{TH}, and a Variable Supply-voltage (VS) scheme [2] is investigated to control V_{DD}. These two research achievements give IC designers freedom of controlling V_{DD} and V_{TH} for better trade-offs between power and speed, while they were given as boundary conditions and unchangeable parameters in conventional design. A RISC core with the VS scheme in VTCMOS is designed. Measured performance in MIPS/W is improved by a factor of more than 2 compared with that of a conventional design, as depicted in Fig. 2. Chip leakage current is controlled for active and standby modes independent of processed V_{TH}, as shown in Fig. 3.

Two MPEG-4 vide codec chips are developed [3][4]. By optimizing V_{DD} and V_{TH}, V_{DD} can be lowered to 2.5V from 3.3V so that power dissipation is reduced by 43%. By employing one more V_{DD}, 1.75V, for non-critical circuits, power dissipation is further reduced by 25%, in total by 55% compared to a conventional design at 3.3V.

Design knowledge on multiple V_{DD}'s and V_{TH}'s are reported in [5] and summarized in Figs. 5 and 6. Power reduction by multiple V_{DD}'s is about 50%. The more V_{DD}'s, the less power dissipation, but the effect will be saturated very soon. Leakage reduction by multiple V_{TH}'s is about one or two orders of magnitude. The leakage reduction effect will also be saturated as the number of V_{TH} increases.

Lowering Capacitance

External memory access consumes considerable power dissipation due to large parasitic capacitance along external signal lines. An MPEG-4 videophone LSI with 16Mbit embedded DRAM is fabricated in a 0.18μm embedded DRAM process [6]. Power dissipation is reduces to one third of the total power dissipation of a two-chip solution, as depicted in Fig. 7.

Lowering Switching Activity

Flip-flops, key circuits to synchronous design, consume large and increasing amount of total chip power dissipation. In a conventional flip-flop, half of the total transistors are subject to consume ac power, even when input data is unchanged. A conditional flip-flop circuit is developed where internal clock is activated only when a new input data arrives [7]. A discrete cosine transform (DCT) block for the MPEG-4 video codec is designed and fabricated with this conditional flip-flop. The chip consumes 24%-51% less power without speed degradation compared to a conventional design, as depicted in Fig. 8.

Conclusion

CMOS power dissipation can be reduced to x0.8-x0.5 by lowering supply voltage, x0.8-x0.3 by lowering capacitance, and x0.8-x0.5 by lowering switching activity. In total, power reduction to x0.5-x0.1 can be achieved by design efforts. Suppose the natural power increase due to device scaling by twice every 6.5 years, this power reduction corresponds to expansion of CMOS life span by about 6-20 years. Even though design challenges should further be taken, such as a better algorithm to lower clock frequency, a new set of technology is strongly required for mass production in the 2010's that can provide a long-term solution to the power problems. It is hoped that innovations will occur as they did before.

Acknowledgement

The author is graceful to T. Shibata for encouragement.

References

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[5] M. Hamada *et al.*, *CICC'01*, pp.89-92, May 2001.
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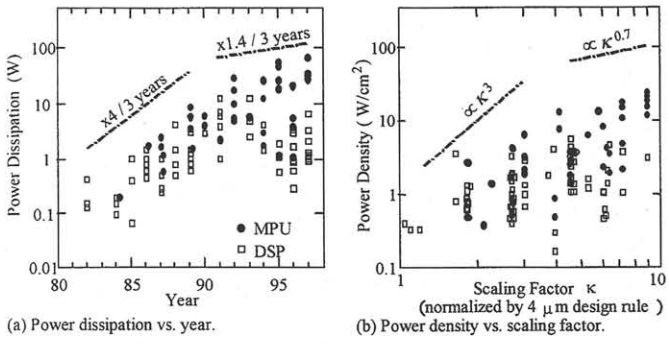


(a) Power dissipation vs. year. (b) Power density vs. scaling factor.

Fig. 1 Power increase due to device scaling.

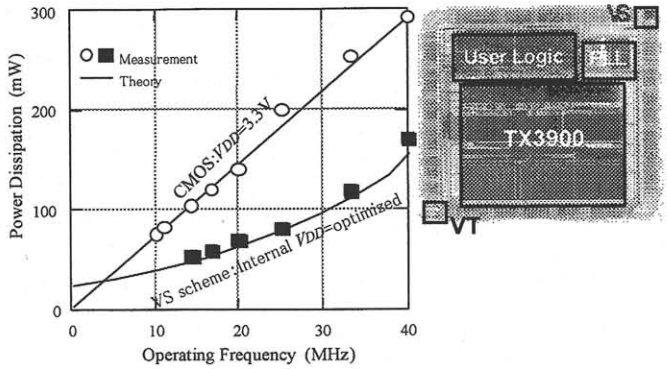


Fig. 2 Power reduction using variable-V_{DD} ,V_{TH} technology.

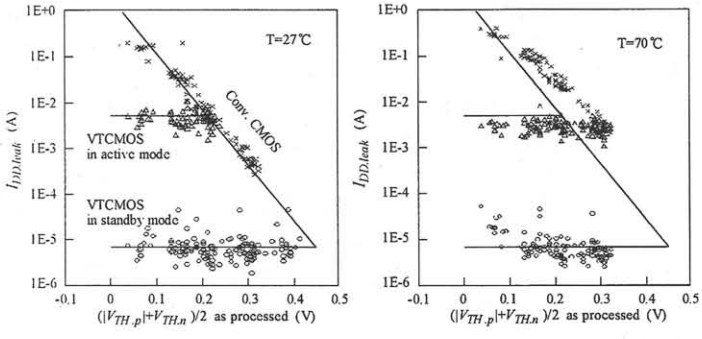


Fig. 3 Chip leakage current in VTCMOS technology.

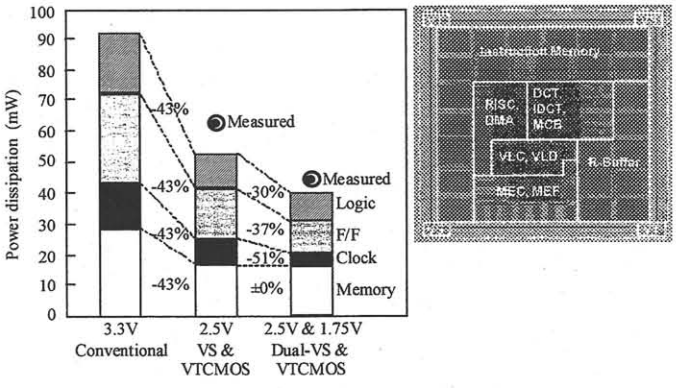


Fig. 4 Power reduction in dual-V_{DD} and VTCMOS technology.

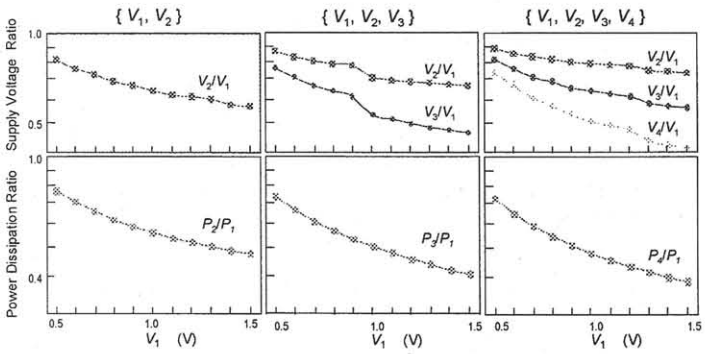


Fig. 5 Optimum multiple-V_{DD}'s for active power reduction.

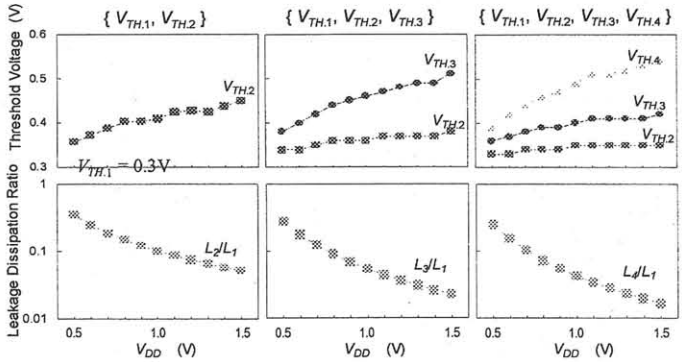


Fig. 6 Optimum multiple-V_{TH}'s for leakage power reduction.

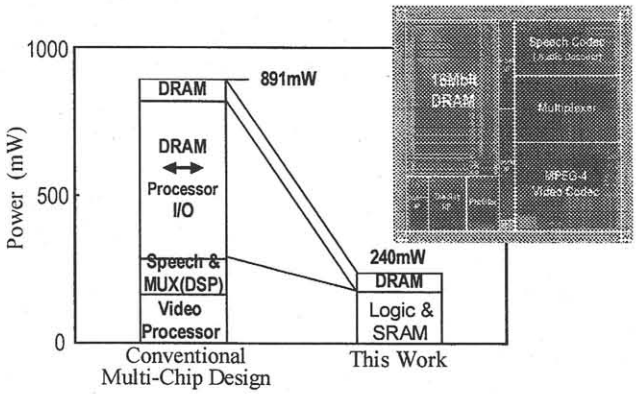
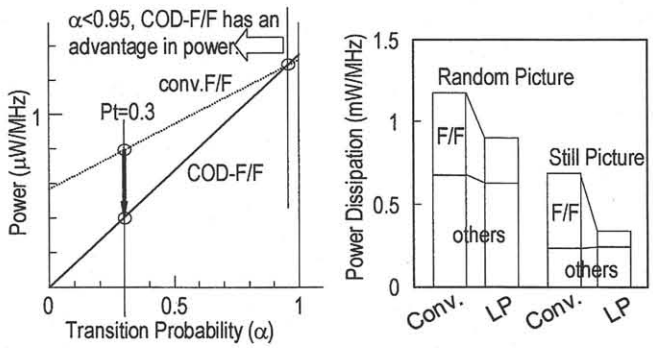


Fig. 7 Embedded DRAM for capacitance reduction.



(a) Power dissipation vs. transition probability. (b) Power reduction in MPEG-4 chip.

Fig. 8 Conditional Flip-Flop for lowering switching activity.