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Low-Power Data-Preserving Complementary Pass-Transistor-Based Circuit for Power-Down Circuit Scheme

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1. Introduction

As a low-power and high-speed circuit technique, multi-threshold voltage CMOS (MTCMOS) circuit scheme is very effective method, which involves using high-V_{th} transistors to switch on or off the power supplies of low-V_{th} logic blocks [1-2]. However, it has a serious problem that the stored data of latch and flip-flop in logic block cannot be preserved when their supply power is turned off (sleep mode). Therefore, extra circuits and complex timing design must be provided for holding the stored data [2]. These cause great penalties of performance, power and area to the system. In another MTCMOS scheme using diode clamp, such as ABC-MTCMOS [3] and VRC [4], the extra circuits in the latches and flip-flops are not required and the control timing design is not complex, but the leakage current of the logic circuits in the sleep mode cannot sufficiently suppressed. In this paper, we propose a new data-preserving latch and flip-flop circuits, called data-preserving Complementary Pass-transistor-based Latch (CPLT) and Flip-flop (CPFF), for power-down circuit scheme. The proposed circuit can preserve its stored data during power-down period while maintaining low leakage current without any extra circuits and complex timing design .

2. Data-Preserving CPLT & CPFF Circuit

The basic circuit diagrams of proposed data-preserving latch and flip-flop circuits in power-down circuit scheme are shown in Figure.1. The circuit configuration and operation principal are similar to the developed complementary pass-transistor-based flip-flop [5]. Basically, they consist of low-V_{th} MOSFETs, except for the latch C1-2, which is high-V_{th} MOSFET and directly connected to real power supply, VDD and GND. The internal clock delay inverter, I3 is a NOR gate with high V_{th} MP1 MOSFET for cut off the leakage current path in sleep mode. The data-preserving CPFF is triggered on the leading edge of the clock. When the clock is L, the latch C1-2 holds the previous data due to N2 and N4 are off. When the clock is H, all N1-4 are turned on for a period determined by inverter I1-3. During this period, input data is sampled into latch C1-2. The low-V_{th} P1-2 directly connected to VDD is for regaining H level and is designed with minimum channel width. Instead of these low-V_{th} P1-2, the latch C1-2 with large PMOS gate width can be also used. Figure 2 shows a timing diagram for active/sleep mode of the proposed circuit. SC is active/sleep switch signal for controlling high-V_{th} power MOSFET. SC_ff is a control signal for latch and flip-flop circuits. In the sleep mode, SC is L and SC_ff is H, and then the N3-4 are turned off. Thus, the data stored in latch can be retained in sleep mode.

The leakage currents of data-preserving CPLT and CPFF in sleep mode is relatively low because only one subthreshold leakage current of low-V_{th} NMOS pass gate (N3 or N4) connected to L level node of C1-2 exits. The leakage current of the NMOS pass gate connected to H level node of C1-2 is very low because its threshold voltage is increased due to substrate-bias effect by increasing of potential of virtual ground, VGND. In a transition from sleep mode to active mode, SC is set to H, then SC_ff is set to L after a delay time (Waiting in Figure 2). This prevents data destruction of the latch, C1-2 when N3-4 turns on. Since the data-preserving CPLT and CPFF are not master-slave type, the transitions of active/sleep mode are independent on the clock state.

3. Simulation Results

To evaluate the performance of the proposed data-preserving circuits, HSPICE simulations with a 0.35 μm CMOS technology were performed at 1.0 V, 85 ℃, f_{clock} = 200 MHz and compared with the conventional flip-flop for MTCMOS (balloon FF [2]) and conventional low-V_{th} TGFF. The flip-flops were designed with 50 fF output load and minimum and maximum gate widths used are fixed to 0.7 μm and 5 μm, respectively. As a power MOSFET for virtual GND, NMOS with W_n=50 μm was used. The low-V_{th} and high-V_{th} of NMOS and PMOS used in the simulation are 0.35 V, 0.6 V and (-) 0.4 V, (-) 0.65 V respectively. Figure 3 shows the delay characteristics of the flipflops. The power consumption of the flip-flop for four different data patterns is also plotted in Figure 4. It is obvious that the data-preserving CPFF is smaller delay and less power compared to conventional flip-flops. Table 1 shows the summarized result of simulated flip-flop and latch characteristics. Figure 5 shows the leakage current comparisons in the case of ten flip-flops. From this result, the leakage current of data-preserving CPFF is as low as that of the balloon flip-flop.

4. Application to 16-bits Telecommunication DSP LSI

We applied the proposed data-preserving circuits to a 16-bits telecommunication DSP LSI containing 72k gate counts. To realize ASIC design, the standard cell library with virtual GND and real GND lines using 0.18 μm CMOS 4-metal technology was developed. In all latch and flip-flop of this DSP LSI, the proposed data-preserving circuits was used. Figure 6 shows chip layout of the designed DSP LSI. After cell placement and route, PowerMill simulation was performed with RC extraction parameter of virtual GND. From the simulation result, the chip operating at 120 MHz was successfully confirmed. Table 2 shows the features of the implemented DSP LSI.

Acknowledgments

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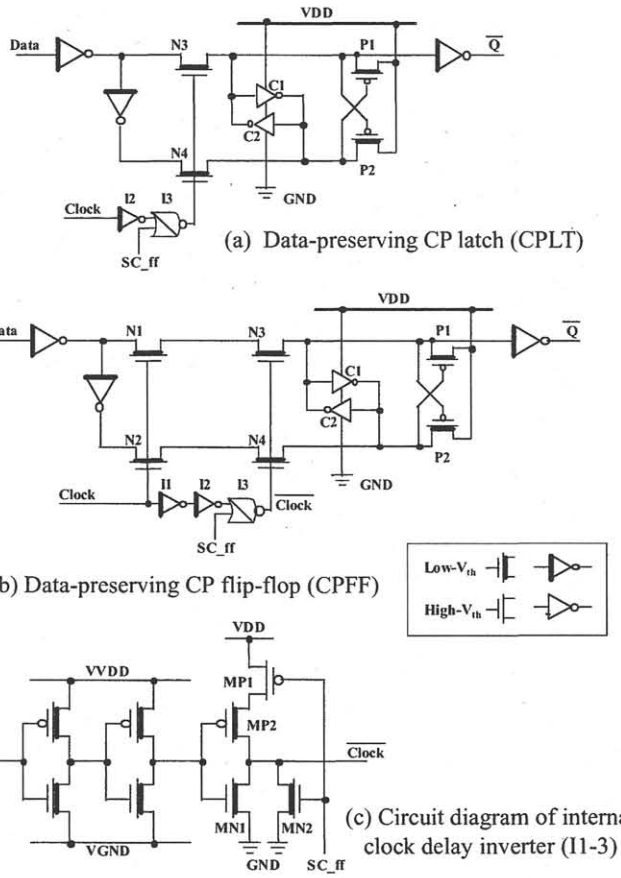

Figure 1. Proposed data-preserving circuits using complementary pass-transistor (CP)

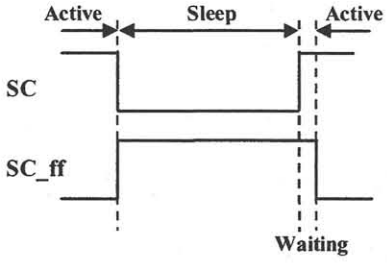

Figure 2. Control timing diagram for Active/sleep mode

Figure 6. Chip layout of DSP LSI

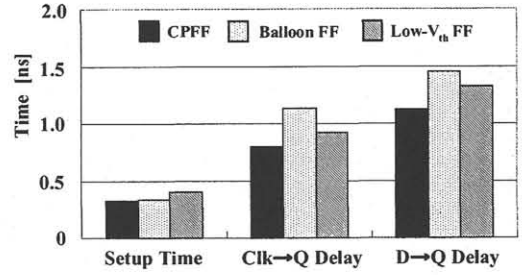

Figure 3. Delay characteristics comparison

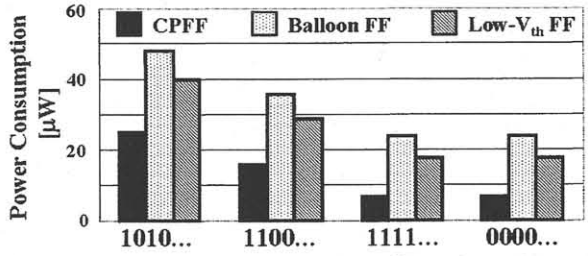

Figure 4. Total power consumption with different input data patterns

	Device Count	Total Gate Width [μm]	Delay [ns]	Total Power [μW]	PDP [fJ]
CPFF	24	43.4	1.11	24.83	25.31
Balloon FF	54	95.9	1.46	47.57	69.44
Low-V_{th} FF	22	57.4	1.32	39.54	52.31

Table 1. Characteristics comparison (1.0 V, 85 ℃, f_{clock} = 200 MHz)

	Device Count	Total Gate Width [μm]	Sleep leakage [pA]
CPLT	20	32.8	472.3
Balloon Latch	28	46.9	105.1
Low-V_{th} Latch	14	32.2	2372.1

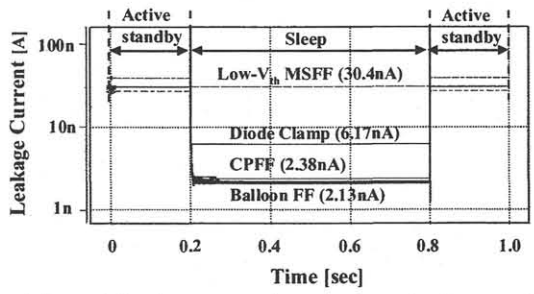

Figure 5. Leakage current comparisons in sleep mode

Table 2

Features of the implemented telecommunication DSP LSI

Technology	0.18 μm CMOS, 4-metal
High-Vth	NMOS: 0.62 V PMOS: (-) 0.62 V
Low-Vth	NMOS: 0.43 V PMOS: (-) 0.43 V
Power supply	1.65 V
Core size	1.0 mm^2
Gate counts	72,000
Power dissipation	59.4 mW