Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 102–103

D-2-3

An Independent-Source Overdriven Sense Amplifier for Multi-Gigabit DRAM Array

Riichiro Takemura, Tomonori Sekiguchi, Hiroki Fujisawa*,
Tsugio Takahashi*, Takeshi Sakata, and Masayuki Nakamura*

Central Research Laboratory, Hitachi Ltd., 1-280,Higashi-koigakubo Kokubunji-shi, Tokyo 185-8601, Japan
Phone: +81-42-323-1111 Fax: +81-42-327-7774 E-mail: r-takemr@crl.hitachi.co.jp
* Elpida Memory, Inc., Sagamihara, Kanagawa 229-1197, Japan.

1. Abstract

We proposed a scheme for an independent-source overdriven sense amplifier that increases the sensing speed of a small signal. The independent-source with distributed drivers eliminates the disturbance from the neighboring sense amplifiers with low power consumption. Under an overdriving voltage of 1.5 V and an array voltage of 1 V, for a retention time of 128 ms, the sensing time by the proposed scheme is expected to be 5 ns, which is better than the 7.3 ns by the conventional distributed overdriven scheme. The proposed scheme will enable 3-cycle t_{RCD} operation at 200 MHz for multi-gigabit DRAM array.

2. Introduction

The increase in power consumption is a serious problem for multi-gigabit DRAMs. The power consumption would be reduced by lowering an array voltage (i.e., data-line swing, VDL), and, in sub-0.1-μm generation, the array voltage is expected to be less than 1.0 V [1]. However, it degrades the read-out signal for sense amplifier (SA), resulting in the sensing speed slower than 5 ns.

A distributed overdriven (D-OD) scheme has been proposed as a way of overcoming this problem [1]. In the D-OD scheme, the sensing time (*tSA*) is improved by applying a higher voltage (VDD) to SAs in the early stage of sensing. Furthermore, the dependence of the *tSA* on the distance from the sense-driver is improved by use of the distributed drivers [2] and meshed power lines [3]. This scheme is promising at operations under a VDL of 1.4 V, but it is insufficient for a VDL of 1.0V. This paper proposes an independent-source overdriven SA that can reduce the signal voltage required for 5-ns sensing.

3. Concept behind Independent-Source Overdriven Sense Amplifier

The problem in the D-OD scheme is caused by the common-source configuration, in which the source nodes of the SAs are connected to common source lines (Fig. 1). In the D-OD scheme, the operation of an SA is disturbed by the neighboring SAs. It is possible to reduce this disturbance by use of the independent-source configuration. The Decoded-source SA (DSSA) scheme [4] improves the *tSA* of the SAs that are selected by column selected line labeled as CSL (Fig. 2). However, this improvement is limited to the column selected SAs. Therefore, the unselected SAs have the *tSA* and the restoring time delayed more than those in the conventional SA, because of the high impedance of series transistors.

The independent-source overdriven scheme can solve the problems in the D-OD and the DSSA schemes (Fig. 3). This scheme separates the source nodes of SAs. This allows us to free both NMOS and PMOS source nodes from the neighboring SAs. The NMOS source node is connected to a sense-driver, which solves the impedance problem. The PMOS source node is connected to an over-driver and a restore-driver, which solves the voltage drop at the VDL power line. Therefore, the proposed scheme can improve the *tSA* of all SAs.

In spite of the addition of restore-drivers and disconnection of source nodes, the area penalties referred to the D-OD scheme are about 13% in the SA area and only 2% in the total chip area, in the case of 4 Gb DRAMs.

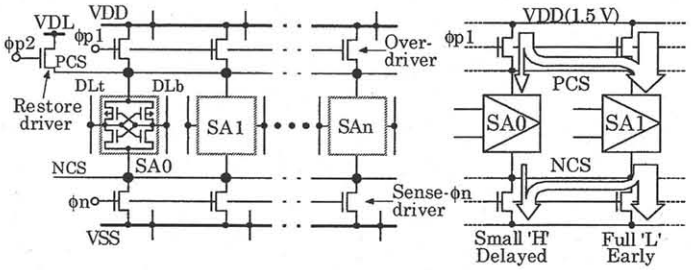

Fig. 1 Circuitry and current flow in the D-OD scheme.

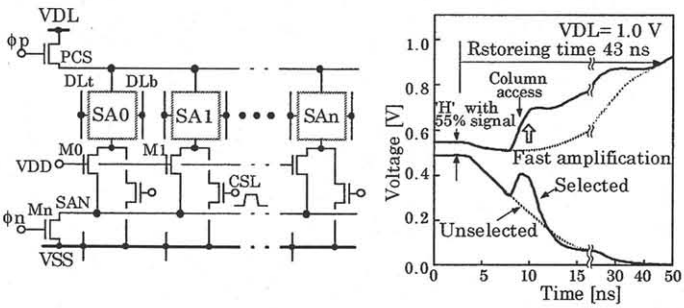

Fig. 2 Circuitry and waveforms of the DSSA scheme [4].

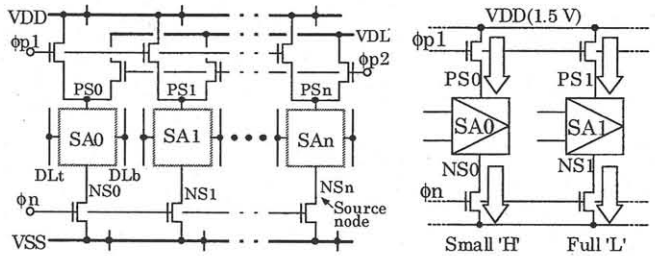

Fig. 3 Circuity and sensing current flow in the proposed scheme.

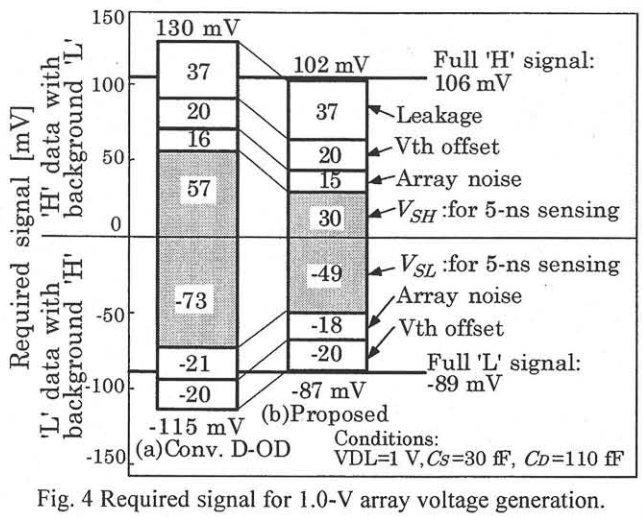

Fig. 4 Required signal for 1.0-V array voltage generation.

4. Simulation

We estimated the required signal voltage for a VDL of 1.0 V (Fig. 4) by circuit simulations. The parameters used for the simulation are as follows; a cell capacitance C_S of 30 fF, a data-line capacitance C_D of 110 fF, and a retention time of 128 ms. We assumed the worst cell leakage of 40 fA, while the cell leakage in the 0.2-μm generation was 20 fA [5]. Based on these parameters, we also assumed (1) the signal loss by the charge leakage of 37 mV, (2) the signal loss by the Vth offset in SA transistors of 20 mV, and (3) the signal loss by the array noise of 16 mV for high data ('H') and 21 mV for low data ('L').

We found that the D-OD scheme would require 57 mV for the 'H', and 73 mV for 'L' in 5-ns sensing (V_{SH} and V_{SL} in Fig. 4), and the total required signal voltages are estimated to be 130 mV for 'H' and 115 mV for 'L'. The available signal voltages are also calculated to be only 106 mV for 'H' and 89 mV for 'L', which, however, are smaller than the values required in the D-OD scheme. This means that the *tSA* in the D-OD scheme becomes greater than 5 ns

Figure 5 shows the simulated waveforms of the data-lines and current of SAs with a full 'L' signal and a degraded 'H' signal (55% signal). The start of sensing by an SA with a full signal (SA1) is faster than an SA with degraded signal (SA0). During the amplification of SA1, the PMOS common source (PCS) level is clamped by the current supplied to SA1, which results in much smaller current supplied to SA0. This leads to *tSA* of 6.8 ns for the degraded 'H' signal sensing.

Figure 6 shows the simulated waveforms in the proposed independent-source overdriven scheme. Even if the start of sensing by SA1 is faster than SA0, the neighboring PMOS-source level (PS0) is not clamped by the current supplied to SA1. The simulated PS0 is higher than PS1 by 50 mV, and therefore, the current supplied to SA0 increases during the early stage of sensing. As a result, the *tSA* for the 'H' with a degraded signal was about 4.6 ns, which is faster than that of the D-OD scheme by 2.2 ns.

We found that the restoring time is 7 ns, which achieves 90% of the VDL for 'H'. This time is better than those in the D-OD and the DSSA schemes by 1 ns and 36 ns, respectively. This satisfies the target of row cycle time of 45 ns.

We also obtained the dependence of the sensing time on the sensing signal (Fig. 7). In the D-OD scheme, the 'H' sensing in 5 ns needs a signal of 57 mV in the worst case, which results in only 46 ms for t_{RET}. The slower sensing is mainly due to the disturbance by the next-neighboring SAs. This is because the *tSA* with only the next-neighboring SA is almost same as that with the SAs in a row (512-SAs/source). The signal required in the proposed scheme is only 30 mV, which, in turn, results in t_{RET} more than 128 ms. The signal required for the 'L' in the worst case is also reduced to 49 mV, which is smaller than that in the D-OD scheme by 24 mV as shown in Fig. 7 (b).

5. Conclusions

We proposed a scheme for an independent-source overdriven sense amplifier that increases the sensing speed of a small signal by suppressing the disturbance from the neighboring SAs. It can reduce the minimum signal required to achieve the 5-ns sensing by 27 mV for 'H' and 22 mV for 'L'. It can also reduce the restoring time by 1 ns. This scheme will enable the DRAM arrays in next generation to operate at 200 MHz (t_{RCD}=15 ns) with an array voltage of 1 V and retention time of more than 128 ms.

6. Acknowledgments

The authors thank Katsutaka Kimura, Shin'ichiro Kimura, Kazuhiko Kajigaya, Satoru Hanzawa, Norikatsu Takaura, Hideyuki Matsuoka, Takayuki Kawahara, Kazuyuki Miyazawa, and Kiyoo Itoh for their fruitful discussions and encouragement.

7. References

[1] T. Takahashi et al., *ISSCC Dig. Tech. Papers*, 2001, pp. 380-381.

[2] H. Hidaka et al., *IEEE J. of Solid-State Circuits*, vol. 27. no. 7, pp. 1020-1027, July 1992.

[3] T. Yamada et al., *IEEE J. of Solid-State Circuits*, vol. 26, no. 11, pp. 1506-1510, November 1991

[4] J. Okamura et al., *IEEE J. of Solid-State Circuits*, vol. 25, no. 1, pp. 18-23, January 1990

[5] K. Saino et al., *IEDM Tech. Dig.*, 2000, pp 837-840.

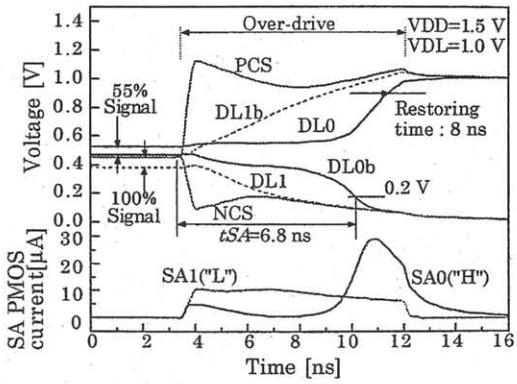

Fig 5 Simulated waveforms of the D-OD scheme.

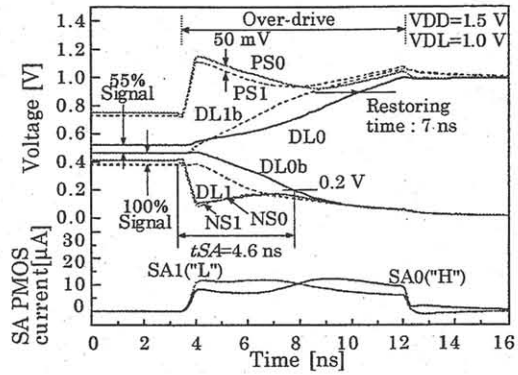

Fig. 6 Simulated waveforms of the proposed scheme.

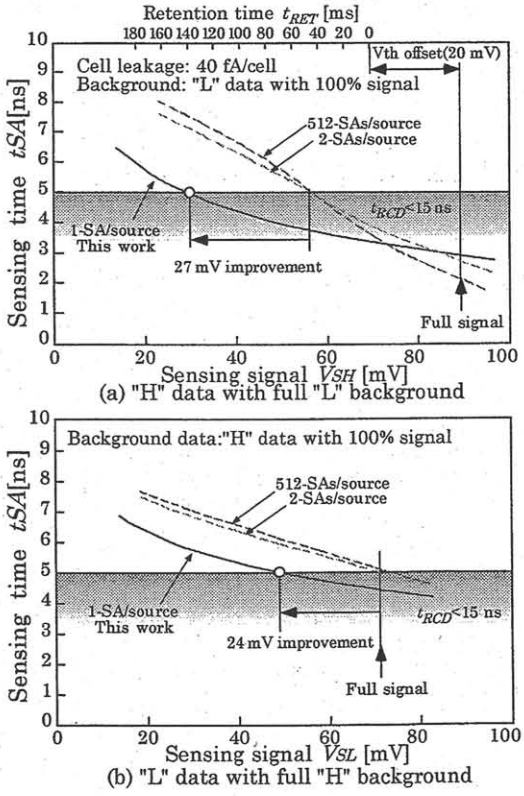

Fig. 7 Dependence of the sensing time on sensing singals.