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Gain-Boosted Operational Amplifier for Low Supply Voltage

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1.Introduction

Switched-capacitor circuits demand the use of high gain Opamps to reduce the effects originating from gain error, for which gain boosting technique has been widely employed. However, the gain-boosted fully differential Opamps require common mode feedback circuits in auxiliary amplifiers which consist of many transistors and capacitors to adjust the output common mode level. Large number of element devices naturally results in the decrease of the operating speed as well as the increase of occupation area. The aim of this work is to propose a gain-boosted Opamp for low supply voltage with auxiliary amplifiers composed of MOS transistors which ensures high speed operation and small die area.

2.Issues of conventional Gain-boost Amplifier

Figures 1 and 2 show the schematic of a telescopic operational amplifier together with its bias circuit. Each bias voltage shown in Fig.2 is corresponding to that depicted in other Figures. Improved NMOS and PMOS input auxiliary amplifiers are employed in this telescopic Opamp. The right-half-plane zero is eliminated by inserting a MOS transistor in series with the compensation capacitor. A simple implementation of gain boosting

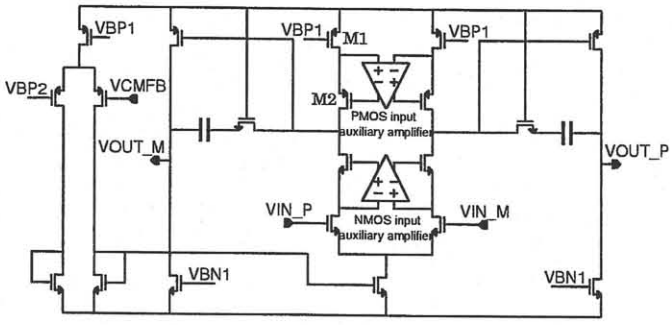

Fig. 1: Conventional gain-boosted telescopic amplifier. Triangles in the center represent auxiliary amplifiers

technique shown in Fig.3 limits the range of output voltage swing because the drain voltage of $M1$ should be larger than overdrive voltage plus threshold voltage of p-ch MOSFETs used, resulting in the fatal problem in low voltage operation. The drawback can be alleviated by employing a folded-cascode circuit shown in Fig.4 since the drain voltage of $M1$ can be reduced as low as its overdrive voltage. In addition, the folded-cascade amplifier significantly reduces Miller effect, leading to high speed operation. However, for fully differential configuration, common mode feedback circuits to adjust the output voltage are required. This is one of the complicated parts of fully differential Opamp design. Conventional common mode feedback circuit utilizes either switched-capacitor or continuous time circuits which require at least 10 devices (capacitors and MOSFETs) except for its bias circuit.

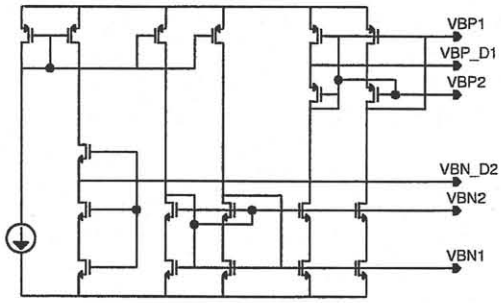

Fig. 2: Bias circuit

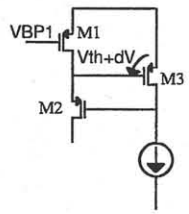

Fig. 3: Simple implementation of gain boosting

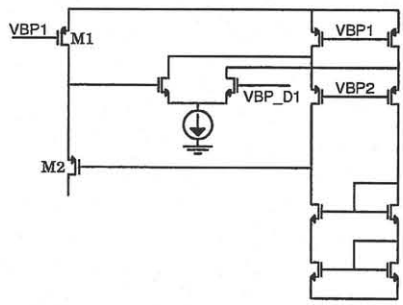

Fig. 4: Folded-cascode gain-boosting amplifier

3.Improved auxiliary amplifier

Figure 5 shows the improved NMOS input auxiliary amplifier designed for our high gain Opamp, which eliminates switching noise arising form the common mode feedback circuits using switched capacitors. In what follows, we explain the NMOS input auxiliary amplifier but not PMOS amplifier because of their complementary

functions. A source-follower is placed between the input node INP and the input gate of M3 to shift the input signal upward. The same size source-follower is also used for the INM counter part. The source-followers make it possible for the differential pair to operate even at low input voltages, INP and INM. The gate of transistor Mb is connected to the bias voltage of VBN-D2 in such a way that the common mode voltage of the NMOS inputs of the auxiliary amplifier shown in Fig.1 stays around VBN-D2. Thus, the output voltages of the auxiliary amplifier are kept in a desired voltage of VBN2. Two MOS capacitors with one-half size of the input MOSFETs M3, M4 are cross-connected between the drains and gates of the input MOSFETs to decrease the Miller capacitance and to achieve high speed operation. Figure 6 shows the

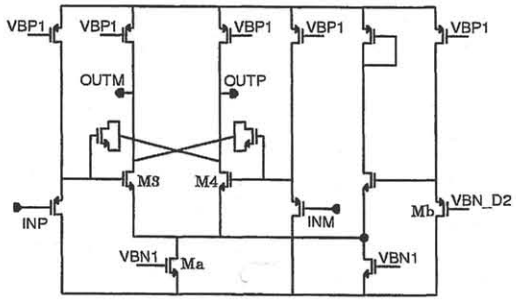

Fig. 5: NMOS input auxiliary amplifier represented as the lower triangle in the high gain Opamp shown in Fig.1

AC response of the improved auxiliary amplifier, which demonstrates a open-loop low-frequency gain of about 30dB and a high unity gain frequency of 356MHz with a 0.35 micron process. The power dissipation of the NMOS input auxiliary amplifier is only 1.1mW. Note that the

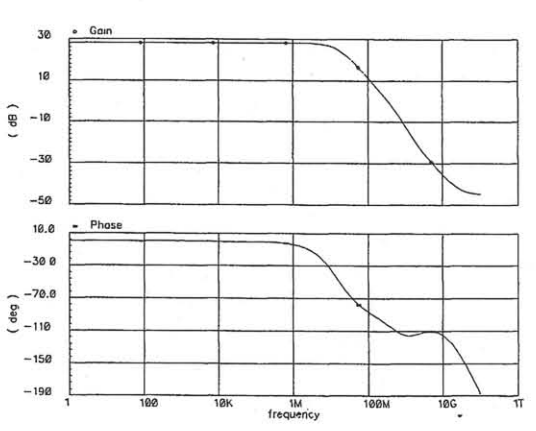

Fig. 6: Open-loop AC response of the NMOS input auxiliary amplifier

dominant pole of the auxiliary amplifier is located at very high frequency so that the settling time of the over all gain-boosted Opamps remains unchanged: As long as its dominant pole is greater than the pole of the Opamps without enhancement, the settling behavior of the gain-enhanced Opamps is not affected.

4.Simulatioin result

Table 1 summarizes the simulated results of the designed Opamp at the supply voltage of 2.7~3.3V. A dc open-loop Opamp gain of 100~109dB and a large phase margin over 60 degree are realized at a mid-supply voltage range regardless of the 10% fluctuation of supply voltage and the variations (SS, TT and FF) of the device characteristics due to fabrication processes. The output

Table 1: Simulation results of the Gain boost Amplifier designed with 0.35 micron CMOS process

Parameter	Simulation results		
supply voltage	2.7V (SS)	3.0V (TT)	3.3V (FF)
DC open-loop gain	109dB	107dB	100dB
unity-gain frequency	107MHz	149MHz	220MHz
phase margin	76	73	67
Power Dissipation	10.8mW	15mW	19.8mW

stage consumes three fifth of the total power dissipation to drive the load capacitance of 3pF connected to the output stage.

5.Conclusions

We designed the auxiliary Opamp composed of MOS transistors only, which makes continuous-time operation possible. Several critical nodes are biased correctly by using source-followers to shift internal voltages upward for low voltage operation. The proposed Opamp can be designed much smaller than conventional auxiliary Opamps using common mode feedback circuit with switched capacitors. The Opamp can be also employed as a high precision buffer because it does not generate any switching noise during operation. The layout of the proposed telescopic Opamp with a $0.35\mu m$ CMOS process has been submitted to the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo.

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